SEMIKRON
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Application Note
AN 17-001

Revision:	00
Issue date:	2017-01-27
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Keyword: SEMIX, SKYPER, press-fit, parallel, current sharing, central driver, individual driver, jitter, common emitter, delay time

IGBT Modules in Parallel Operation with Central and Individual Driver Board

1. General

Parallel circuits are always necessary when the performance criteria of a single component are insufficient. This starts at the microscopic chip level with several 100,000 individual IGBT cells, then further in the module by the parallel connection of chips and continues at the circuit level by parallel connection of modules and entire inverter units. [2]

Maximum utilization of the switch unit resulting from parallel connection is achieved only with ideal static (i.e., during the conduction period) and dynamic (i.e., during the switching period) symmetry of the current. [2]

This application note gives an overview of the causes that can be attributed to an asymmetrical current distribution. It also serves as an aid to the effective parallel connection of IGBT power modules. The focus is on the influence of the driver concept used (individual or central driver) as well as the impedances contained in a system.
For further information, please refer to the SEMIKRON® "Application Manual Power Semiconductors" [2].

2. Definition of Terms

Static current distribution

In this application note, the static current distribution is the current distribution during the common conducting phase of the parallel semiconductors or modules.

Dynamic current distribution

In this application note, the dynamic current distribution is to be understood as the current distribution during the switching operation of the parallel semiconductors or modules.

3. Essential Factors Influencing Asymmetrical Current Distribution

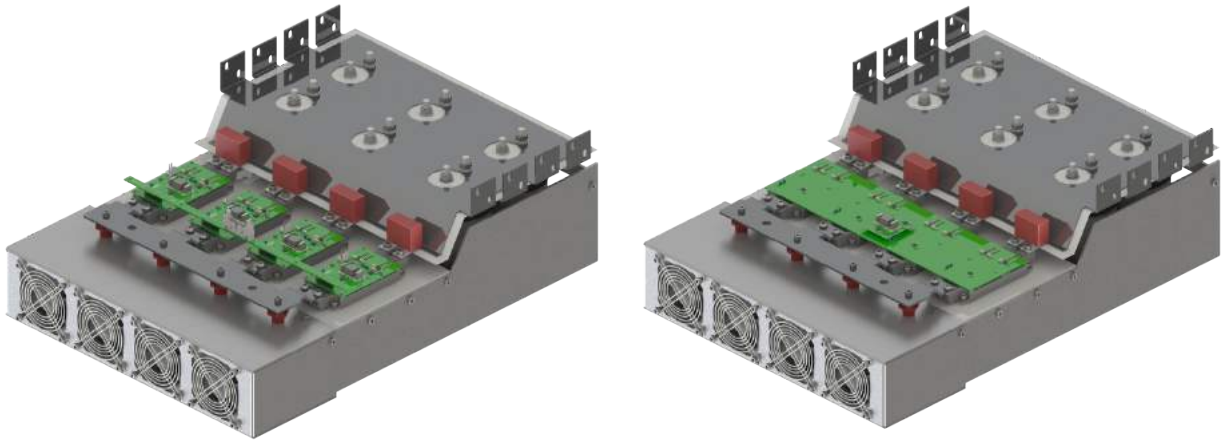
Table 1: Factors influencing asymmetrical current distribution

		Static current distribution	Dynamic current distribution
Semiconductor	Saturation voltage $V_{CEsat} = f(i_C, V_{GE}, T_j)$ $V_F = f(i_F, T_j)$	x	
	Transfer characteristics $I_C = f(V_{GE}, T_j) g_{fs}$ $V_{GE(th)}$		x
	Internal gate resistors $i_C = f(V_{GE}(t))$		x
Module	Stray inductance of the commutation circuit L_σ		x
Driver	Jitter		x
	Cycle time		x
	Gate voltage (supply) $i_C = f(V_{GE}(t))$	x	x
Driver circuit	Stray inductance Gate $L_{\sigma G}$ $i_C = f(V_{GE}(t))$		x
	Stray inductance Emitter $L_{\sigma E}$ $i_C = f(V_{GE}(t))$		x
	Gate resistors $i_C = f(V_{GE}(t))$		x
	Emitter coupling, with shared emitter path		x
Design	Load circuit impedance	x	
	Cooling conditions $I_C = f(V_{GE}, T_j) g_{fs}$	x	

4. Experimental Setup

The investigations regarding the current distribution were carried out on a phase module, consisting of four SEMIX®603GB12E4p modules connected in parallel. Figure 1 shows the individual driver concept on the left and the concept with a central driver on the right-hand side.

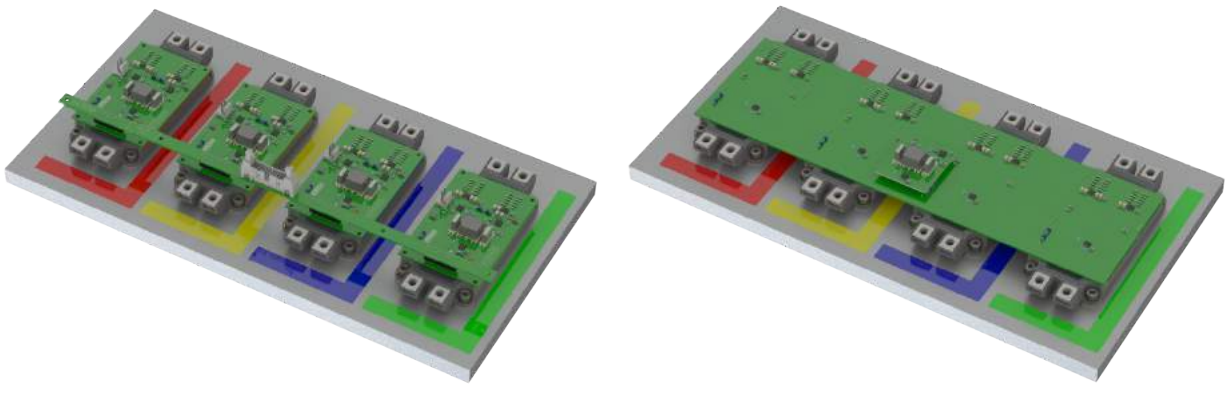
Figure 1: Phase module with individual drivers (left) and central driver (right)



The individual driver concept is based on the SKYPER12 press-fit driver especially developed for the SEMIX® press-fit module. Each of the four drivers has its own primary and secondary side with its associated output stage. Every one of the output stages controls one of the four parallel SEMIX®603GB12E4p modules. The four individual drivers are connected on the primary side via an adapter board, which interfaces the signals from the higher-level control unit to the individual drivers.

The core of the concept with the central driver is a SKYPER® 42 LJ R, which is directly connected to the higher-level control unit. An adapter board serves as an interface to the four SEMIX® modules. On this board are located the gate and emitter resistors as well as the gate protection circuits. Each module switch has its own gate circuit, which is controlled by the central secondary stage of the SKYPER® 42 LJ R.

Figure 2: Modules with individual drivers (left) and central driver (right)



The coloured markings of the module positions in Figure 2 serve as an orientation aid. They correspond to the colours of the traces in the diagrams of this application note.

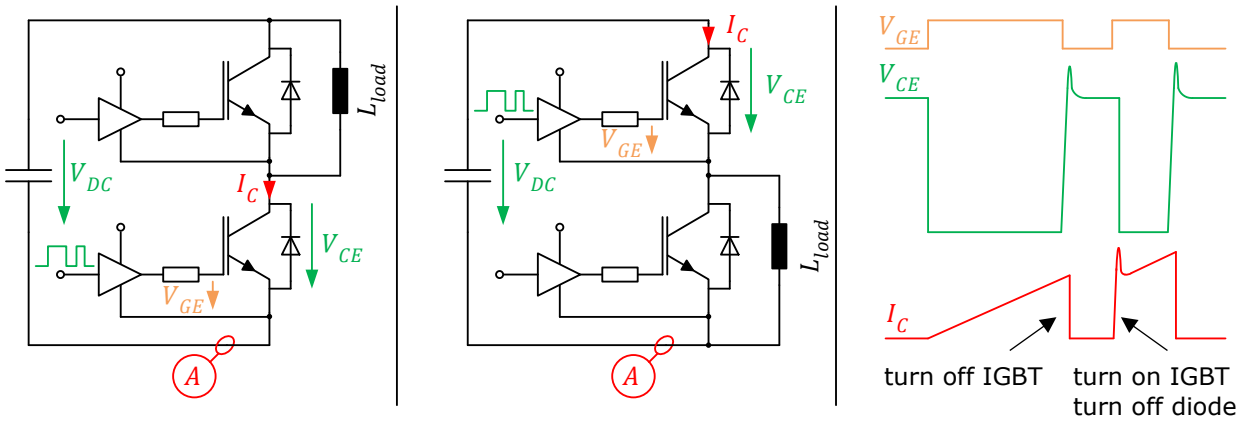
5. Measurement Method

The influence of the various factors on the current distribution was determined using two different measuring methods. On the one hand, the double pulse method, which is well suited for characterising the switching behaviour of semiconductors. On the other hand, the inverter operation, which maps the load of the semiconductors or modules in close reference to the application.

5.1 Double pulse test

Figure 3 shows the basic setup of the double pulse test for the BOT IGBT (left) and the TOP IGBT (middle). During this measurement the corresponding IGBT is switched on and off twice. At the end of the first pulse, the turn-off behaviour can be characterised, at the beginning of the second pulse the turn-on behaviour of the IGBT.

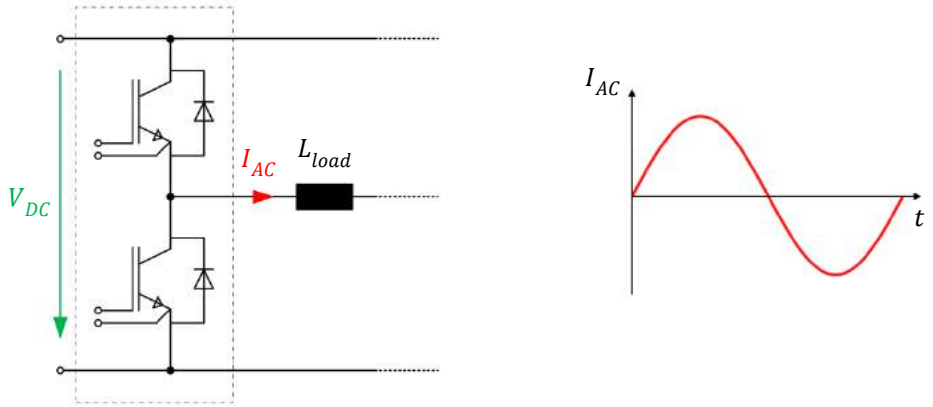
Figure 3: Functional diagram of the double pulse test



5.2 Inverter operation

The inverter operation was carried out in a single phase, H-bridge configuration with an inductive load. In contrast to the double pulse method, in the inverter mode the semiconductors are continuously controlled via a pulse-width-modulated signal. The temperature dependency of the power semiconductors is to be considered as an additional influencing factor on the current distribution during inverter operation.

Figure 4: Functional diagram of the inverter operation



5.3 Test conditions

Table 2: Test conditions for double pulse test and inverter operation			
Letter symbol	**Double pulse test**	**Inverter operation**	**Unit**
T_j	125	---	[°C]
T_{sense}	---	80	[°C]
$I_{C,sum}$	2400	---	[A]
I_{AC}	---	1000	[A]
V_{CE}	600	---	[V]
V_{DC}	---	600	[V]
$V_{G(on)}$	15	15	[V]
$V_{G(off)}$	-8	-8	[V]
f_{sw}	---	3	[kHz]
L_{load}	30 (15)	250	[µH]

6. Influence of the Impedances on the Current Distribution

The impedances contained in a system and thus the mechanical design of the system bears considerable influence on the current distribution between parallel connected modules. The reasons for this are, on the one hand, the differences in the impedance values of the individual current paths, which result from the asymmetry of the design. On the other hand, the spatial position of the individual components relative to each other and the resulting inductive couplings influence the current distribution.

By choosing a smart design, the effects of the influencing factors can be significantly reduced. The more symmetrical the structure of the system, the more symmetrical is the current distribution.

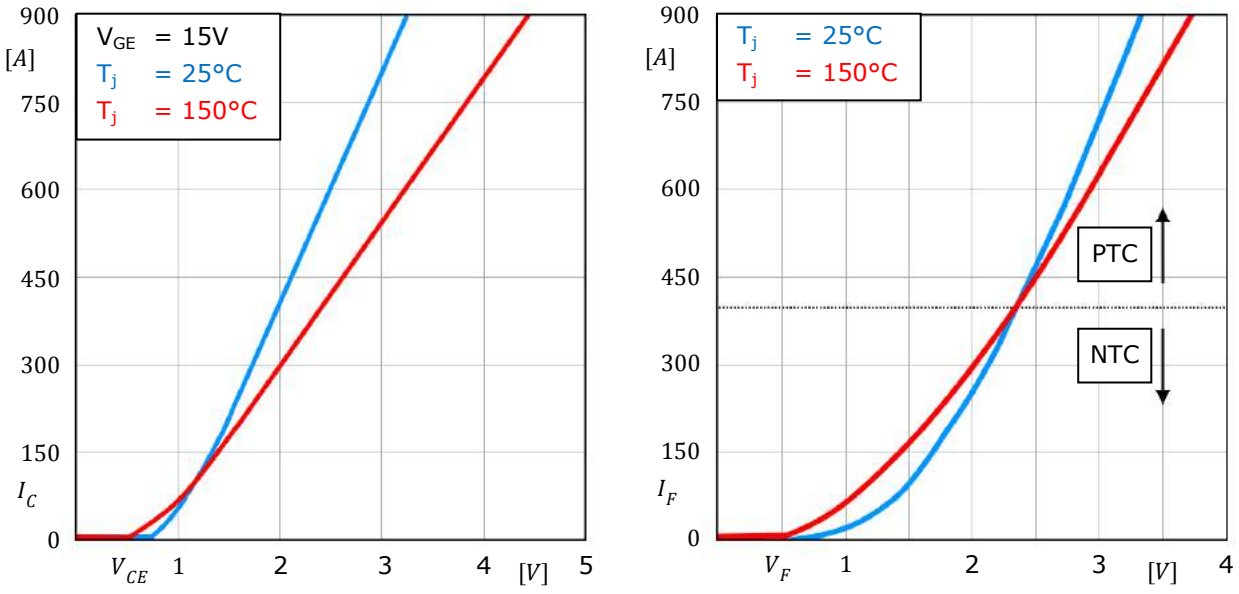
In this chapter the influence of the system design is considered independently of the driver concepts. The influences that the mechanical design exerts only in connection with one of the two driver concepts are explained in chapter 7. The measuring results shown below are determined using the individual driver setup, but are valid for both driver concepts. For the theoretical considerations, it is always assumed that only semiconductors or modules with identical characteristics are connected in parallel.

6.1 Static current distribution

In this application note the influence of the parasitic inductance of the load circuit on the current distribution is investigated. For the sake of completeness, however, the effect of differences in the forward voltage is also to be mentioned:
Modern IGBTs have a positive temperature coefficient (PTC). That is, the saturation voltage increases with the temperature at the same current. This has a pro-symmetrical effect: The IGBT, which takes more current because of lower forward voltage, becomes warmer, the saturation voltage increases and the current is transferred to the parallel IGBT.
Most diodes are considered to have a negative temperature coefficient (NTC) in their rated current range. This behaviour leads to higher current asymmetry than with PTC characteristic. It may be sensible to select diodes according to the forward voltage V_F for the parallel circuit.

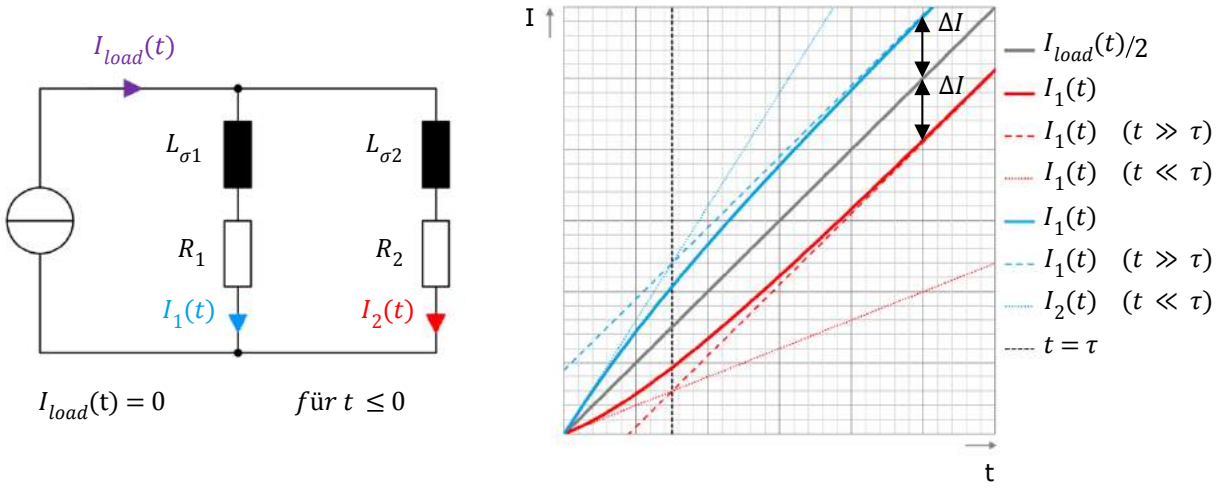
The static and also dynamic differences are minimised for chips within a given production lot, as they have been manufactured from similar silicon under the same manufacturing conditions. Therefore, it is wise to select modules with similar date codes for paralleling.

Figure 5: IGBT V_{CEsat} characteristic (450A nominal current, left)
Diode V_f characteristic (450A nominal current, right)



The influence of the parasitic inductances is described mathematically by means of the simplified equivalent circuit diagram shown in Figure 6. It consists of two parallel current paths and a current source from which the current $I_{load}(t)$ flows. $L_{\sigma 1}$ and $L_{\sigma 2}$ represent the sum of all parasitic inductances of a current path, R_1 and R_2 represent the sum of all ohmic resistances.

Figure 6: Equivalent circuit diagram of two parallel current paths



In order to describe the current distribution with the terms listed below, three assumptions must be made.

(1) The rising current dI_{load}/dt is constant during the common conductance phase of the IGBTs and is determined by the behaviour of the current source V_1.

(2) The influence of the ohmic resistances on the current distribution is negligible $R_1 = R_2 = R$.

(3) The load current $I_{load}(t)$ is zero for the period $t \leq 0$ [3].

$$I_1(t) = \frac{I_{load}(t)}{2} - \Delta I \cdot \left(1 - e^{-t/\tau}\right) \qquad I_2(t) = \frac{I_{load}(t)}{2} + \Delta I \cdot \left(1 - e^{-t/\tau}\right) \qquad with: \quad \Delta I = \frac{L_{\sigma1} - L_{\sigma2}}{4R} \cdot \frac{dI_{load}}{dt}$$

$$\tau = \frac{L_{\sigma1} + L_{\sigma2}}{2R}$$

$$I_1(t) \approx \frac{L_{\sigma2}}{L_{\sigma1} + L_{\sigma2}} \cdot I_{load}(t) \qquad I_2(t) \approx \frac{L_{\sigma1}}{L_{\sigma1} + L_{\sigma2}} \cdot I_{load}(t) \qquad for: \quad t \ll \tau$$

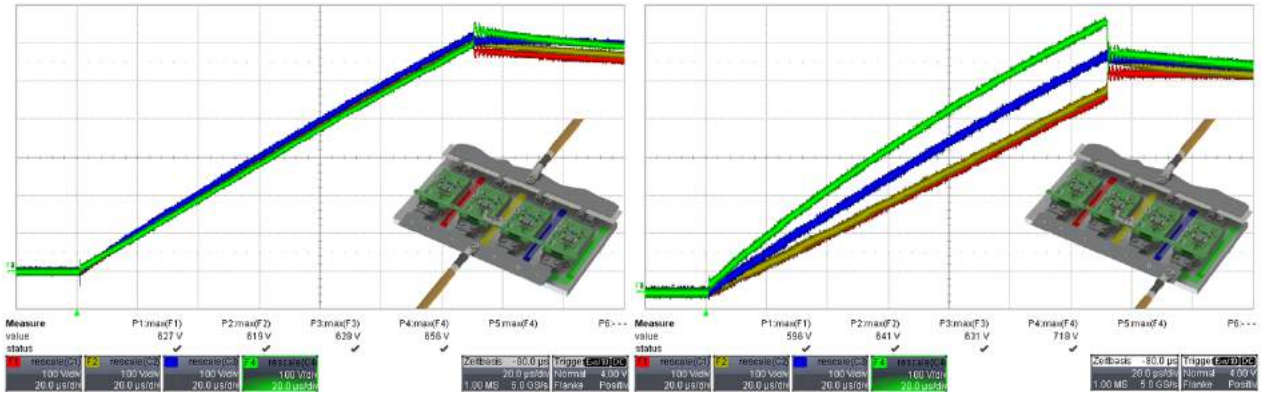
$$I_1(t) \approx \frac{I_{Load}(t)}{2} - \Delta I \qquad I_2(t) \approx \frac{I_{Load}(t)}{2} + \Delta I \qquad for: \quad t \gg \tau$$

The formulas show that the current divider of the branch inductances determines the current asymmetry for times $t \ll \tau$. As the time increased $t \gg \tau$ the two branch currents, at a distance of ΔI, extend parallel to half the load current $I_{load}(t)/2$. The magnitude of ΔI is dependent on the difference of the branch inductances $L_{\sigma1} - L_{\sigma2}$, the sum of the ohmic branch resistances and the current rise time dI_{load}/dt. The current rise time, in turn, in the real application is decisively determined by the level of the DC-bus voltage and the magnitude of the load inductance.

6.1.1 Parasitic inductances

The diagrams shown in Figure 7 show the influence of the parasitic inductances on the static current distribution. Both measurements were performed under identical conditions except for the position of the load cable connector on the AC busbar.
The left diagram shows the current distribution on the four modules, for the case of the load connected centrally to the AC busbar. The right diagram shows the current distribution for the case of an off-centre connected load to the AC busbar.
The variation of the load connection changes the absolute magnitudes of the parasitic inductances as well as their relationships to each other. The current path, which is furthest away from the common load connection, has the largest inductance; the current path closest to the common load connection shows the lowest inductance. The resulting asymmetrical, inductive current divider, in this case, causes an increase of the current through the right module of approximately 20%, referenced to the nominal current $I_{C,sum}/4$.

Figure 7: Measurements of the influence of parasitic inductances



IGBT turn on; AC current; 100A/div; 20µs/div

IGBT turn on; AC current; 100A/div; 20µs/div

6.1.2 Load inductance

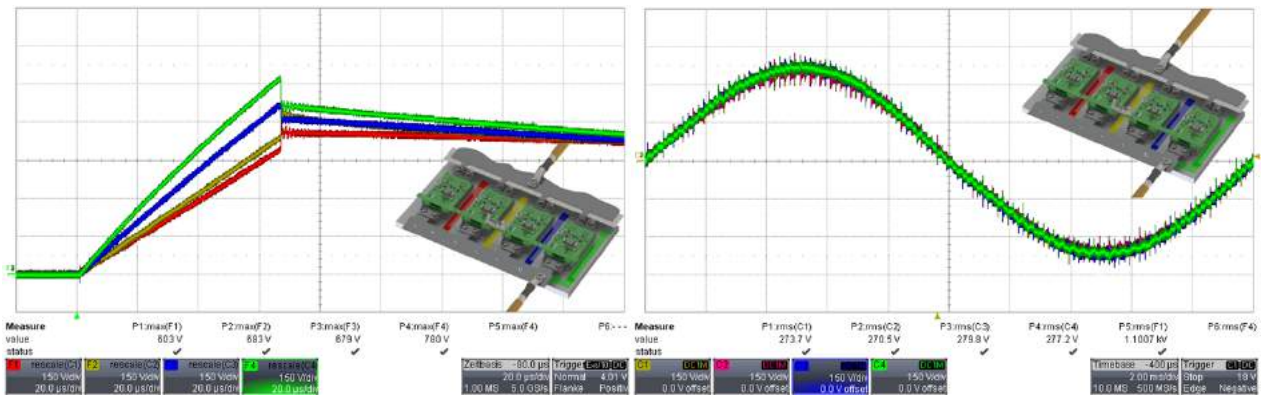
In addition to the parasitic inductances, the size of the load inductance also influences the symmetry of the current distribution. The reason for this is the dependence of the slope of the load current on the load inductance $dI_{load}/dt = {}^{V_{DC}}/_{L_{load}}$. The smaller the inductance of the load, the steeper the increase of the load current and the greater is the asymmetry of the current distribution, in the case of an off-centre load connection.

This must be taken into account when evaluating the results of the double pulse test. This is often carried out using a smaller load inductance than that used in the actual application. An inverter test under appropriate application relevant conditions is the better evaluation basis for the current distribution in normal operation. In addition, the semiconductors heat up due to the continuous load during the inverter operation. Depending on the chosen operating point and on the external cooling conditions, different junction temperatures result in the semiconductors, which in turn influences the current distribution.

The left oscillogram in Figure 8 shows the current distribution with the double pulse test with a load inductance reduced to half, compared to the measurement from chapter 6.1.1. (right diagram). As in the case of the measurement from chapter 6.1.1 the load is also connected off-centre here and results in an asymmetrical current distribution. The raise in the current through the right module increases to about 30% from approx. 20% (measurement from chapter 6.1.1) due to the lower load inductance.
Considering the results of the converter operation, however, which was carried out with the same off-centre position of the load connection, an asymmetrical current distribution of only approximately 2% rms relative to the nominal current $I_{AC}/4$, occurs.

Due to the positive temperature coefficient of the IGBT collector-emitter voltage (VCE) and the higher load inductance, the current distribution in the inverter mode is much better than in the double pulse test with a low load inductance.

Figure 8: Measurements of the influence of the load inductance



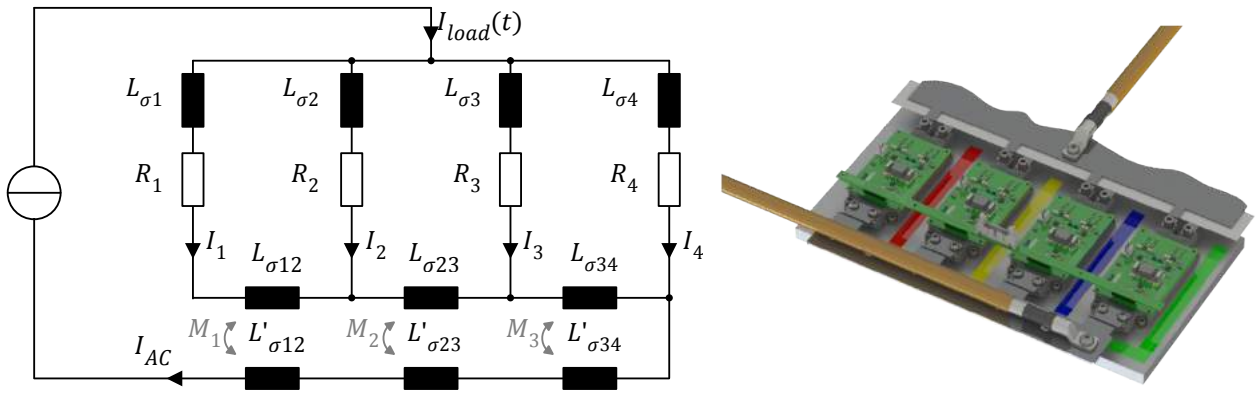
IGBT turn on; AC current; 150A/div; 20µs/div

inverter mode; AC current; 150A/div; 2ms/div

6.1.3 Inductive coupling

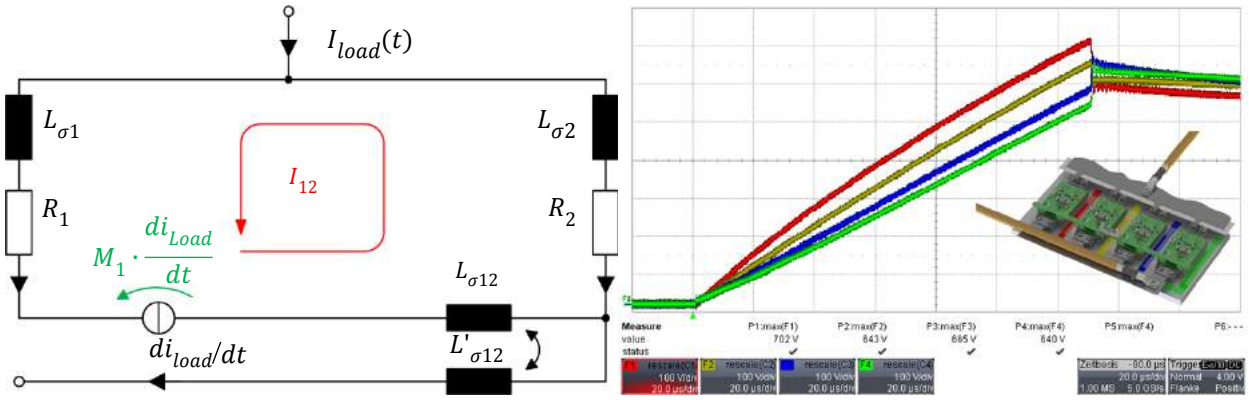
Just as important as a symmetrical design is the arrangement of the current conducting components in the system. An illustration is the example shown in Figure 9, in which the load cable is connected to the right side of the AC busbar. Contrary to the previous measurements, the load cable does not run from the AC-busbar at 90° but in parallel in the immediate vicinity of the AC-busbar and leaving to the left.

Figure 9: Equivalent circuit diagram of four parallel current paths with inductive coupling



Assuming that all inductances depicted in the equivalent circuit have the same value and there is no inductive coupling between the load cable and the AC busbar, the current path with the smallest impedance is located on the right and the current path with the largest impedance on the left side. Accordingly, a current distribution should result corresponding to the right hand trace of Figure 7. The actual current distribution, which results from the inductive couplings M_1, M_2 and M_3 between the load cable and the AC busbar, is depicted in Figure 10.

Figure 10: Influence of inductive coupling



IGBT turn on; AC current; 100A/div; 20µs/div

The equivalent circuit diagram on the left-hand side in Figure 10 is used to illustrate this effect. It shows two parallel current paths with a coupling between the parasitic inductance of the AC busbar $L_{\sigma12}$ and the parasitic inductance of the load cable $L'_{\sigma12}$. The coupling between the two inductances is symbolised by a voltage source with a terminal voltage $M_1 \cdot di_{Load}/dt$.

If a current changing over time flows through $L'_{\sigma12}$ this induces a voltage along the AC busbar due to the inductive coupling. Caused by this voltage, a circular current I_{12} flows counter clockwise through the network consisting of $L_{\sigma1}$, R_1, $L_{\sigma12}$, R_2 and $L_{\sigma2}$. The superposition of the circular current with the load currents leads to the current distribution shown in Figure 10.

The outcome of this effect is proportional to the factor of the inductive coupling. This, in turn, is dependent on the distance between the current-carrying conductors and their position relative to one another. If the distance between the AC busbar and the load cable increases, the coupling factor decreases due to the magnetic field lines becoming weaker with the distance. The effect can be completely eliminated by moving the load cable perpendicularly away from the AC busbar, since the magnetic field lines extend parallel to the AC busbar.

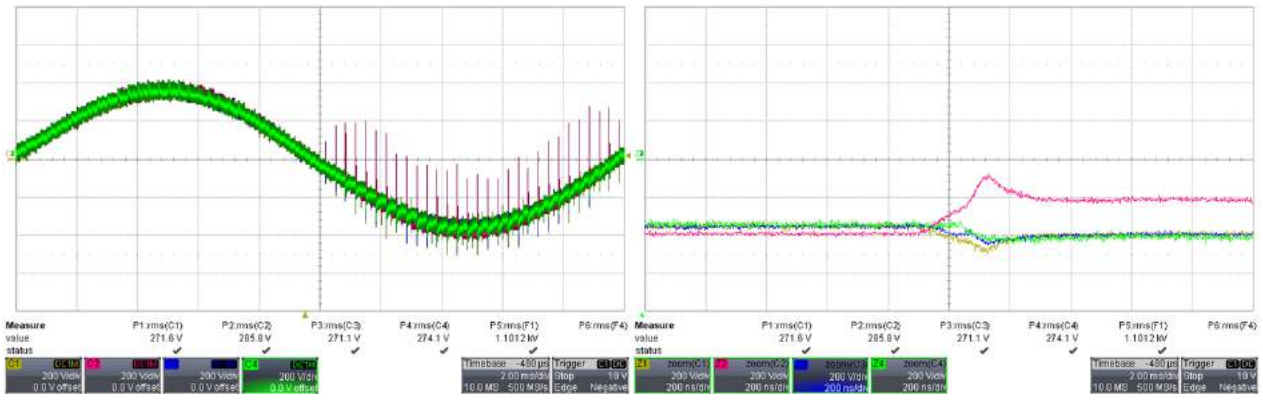
6.2 Dynamic current distribution

Dynamic current distribution is mainly determined by the different switching times of the modules operated in parallel and thus by the characteristics of the drivers, the gate circuit and the semiconductor elements. The mechanical design has a direct influence on the dynamic current distribution only when the commutation sequences take place across the modules. For cross-module commutation processes, the guiding principle applies: "The more symmetrical the mechanical design of the system, the more symmetrical is the current sharing".

This application note is based on the case of module-internal commutation, in which the mechanical design of the system is not the cause for the asymmetrical current distribution but affects the degree of asymmetry.

Figure 11 on the left side shows the typical current profile for modules which are operated in parallel but not exactly simultaneous. To highlight this effect, the BOT switch of a module (red curve) was switched on with a delay of 100ns. The time-delayed switching leads to an asymmetrical dynamic current distribution between the modules in the negative part of the cycle, whereas the current distribution is symmetrical in the positive half-wave. The right side of the figure shows a turn-on sequence of the parallel BOT IGBTs during the negative half cycle of the output current. The IGBT, which last changes from the non-conducting to the conducting state, takes up significantly less current at the beginning of the common conduction phase, since the IGBTs, which turn on first, take over a part of the total current.

Figure 11: Measurement of the influence of different switching time on the dynamic current distribution

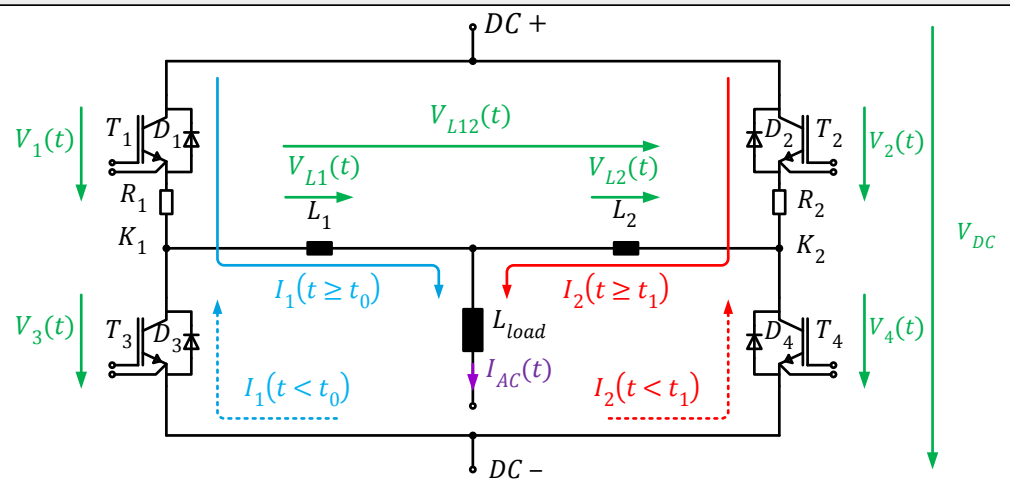


inverter mode; AC current; 200A/div; 2ms/div

inverter mode; AC current; 200A/div; 200ns/div

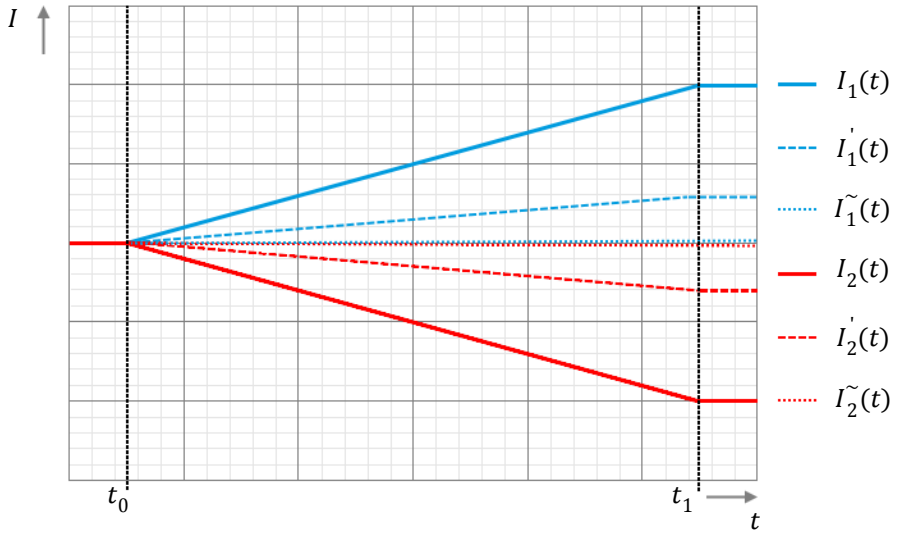
The influence of the mechanical design on the dynamic current asymmetry is described by the equivalent circuit diagram shown in Figure 12. This consists of two parallel connected modules with identical characteristics. L_1 and L_2 symbolise the sum of the inductances, R_1 and R_2 the sum of the resistances which are located in the AC branches. For the sake of simplicity, both L_1 and L_2, as well as R_1 and R_2 have identical values, where: $L_1 = L_2$ and $R_1 = R_2$. L_{load} represent the inductive load of the common AC output through which the total current $I_{AC}(t)$ flows.

Figure 12: Equivalent circuit diagram for two parallel modules



The diagram in Figure 13 shows the calculated current profiles of $I_1(t)$ or $I_2(t)$ for three different values of the inductances L_1 or L_2 respectively. The inductance for the calculation of $I_1(t)$ or $I_2(t)$ corresponds to the value L, for the calculation of $I_1^{'}(t)$ or $I_2^{'}(t)$ to the value $3.3 \cdot L$ and for the calculation of $I_1^{\sim}(t)$ and $I_2^{\sim}(t)$ to the value $67 \cdot L$. The current profiles show a switch on process of IGBT T_1 or T_2 in which IGBT T_1 switches on fist. The calculation is also valid for the switch off process of IGBT T_1 or T_2, but with reverse signs for ΔI.

Figure 13: Current distribution as a function of the inductances L_1 or L_2



The basis for the consideration is a current $I_{AC}(t)$ distributing uniformly to the diodes D_3 and D_4 up to the time t_0.

$$I_1(t) = I_2(t) = \frac{I_{AC}(t)}{2} \qquad for\ t < t_0$$

At the time t_0 IGBT T_1 turns on, diode D_3 takes up blocking voltage and raises the voltage at the node K_1 to the value $V_{DC} - V_1(t)$. Until turn-on of IGBT T_2 at the time t_1 diode D_4 keeps the voltage at node K_2 at $V_{DC} - V_4(t)$. The voltage $V_{L12}(t)$ thus occurs across the inductances L_1 and L_2.

$$V_{L12}(t) = V_{L1}(t) + V_{L2}(t) = V_{DC} - \left(V_1(t) + V_4(t)\right) \qquad for: t_0 \leq t < t_1$$

The voltage $V_{L12}(t)$ leads to a change in the currents $I_1(t)$ and $I_2(t)$, which can be calculated using the following equation.

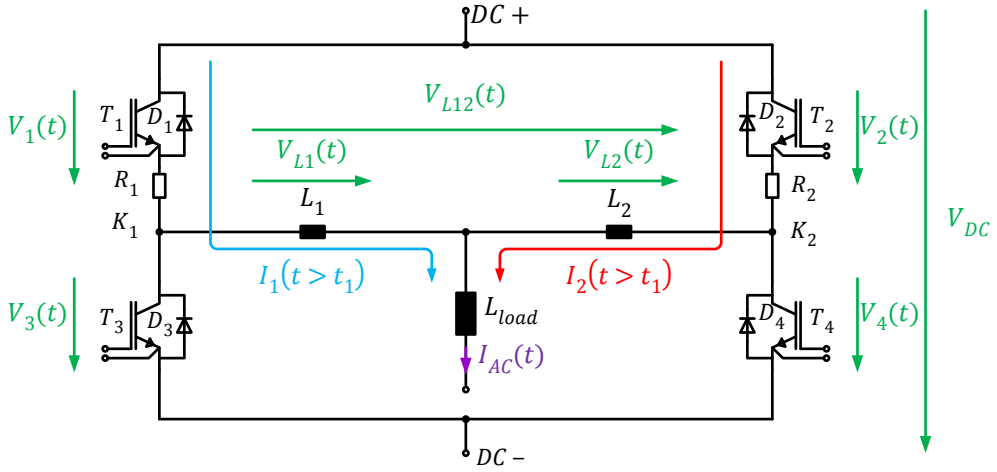
$$I_{1,2}(t_1) = \frac{I_{AC}(t_0)}{2} \pm \frac{U_{L12}(t)}{L_1 + L_2} \cdot (t_1 - t_0) \qquad for: t_0 \le t < t_1$$

The term shows that by introducing additional inductance, for example by means of longer load cables at the AC terminals of the modules, the rise time di_1/dt bzw. di_2/dt can be reduced. Thus, with an identical delay time and an identical voltage drop across the inductances L_1 and L_2, a smaller difference between $I_1(t_1)$ and $I_2(t_1)$ results.

6.3 Current sharing symmetry effect during the common conduction phase of the semiconductors

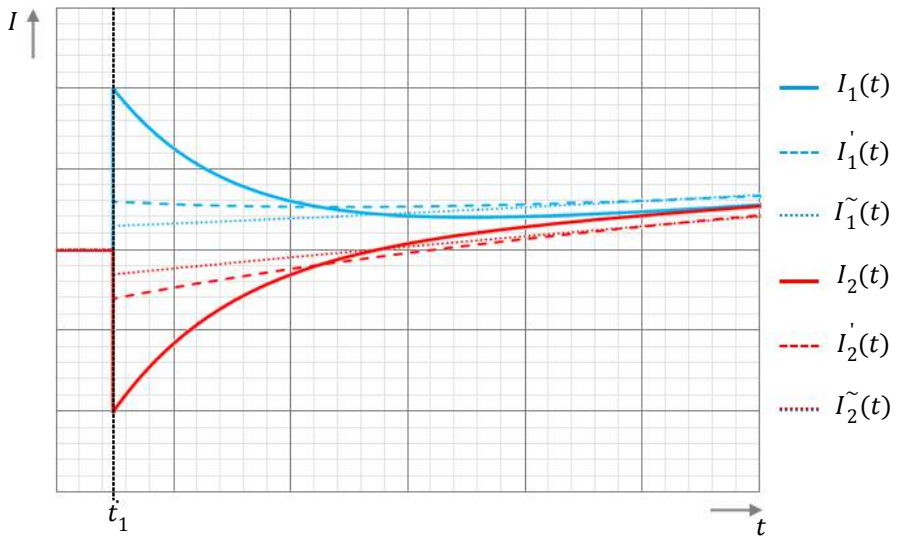
If the current has been unevenly distributed between the parallel current paths during the commutation phase, the currents will completely or partially recombine during the common conducting phase of the IGBTs.
The effect of current sharing is explained below using the example of two identical modules which are operated in parallel. Figure 14 shows the corresponding simplified equivalent circuit diagram, analogue to the one in Figure 12.

Figure 14: Equivalent circuit diagram for two parallel modules



The diagram in Figure 15 shows the calculated current profiles of $I_1(t)$ or $I_2(t)$ for three different values of the inductances L_1 or L_2 respectively. The inductance for the calculation of $I_1(t)$ or $I_2(t)$ corresponds to the value L, for the calculation of $I_1^{'}(t)$ or $I_2^{'}(t)$ to the value $3.3 \cdot L$ and for the calculation of $I_1^{\sim}(t)$ and $I_2^{\sim}(t)$ to the value $67 \cdot L$. The resistance values R_1 bzw. R_2 are identical for all three calculations.

Figure 15: Current sharing symmetry effect as a function of L_1 and L_2 after switching on the IGBTs



The basis for the consideration is that IGBT T_1 turns on first, both IGBTs T_1 and T_2 are turned on at the time t_1 and the currents are divided according to the situation described in section 6.2.

$$I_{1,2}(t_1) = \frac{I_{AC}(t_1)}{2} \pm \Delta I(t_1)$$

The inductances L_1 and L_2 can be neglected at time t_1, the point of inflection of the currents $I_1(t)$ and $I_2(t)$. At the node K_1 a voltage of $V_{DC} - I_1(t_1) \cdot R_1$ will result and at the node K_2 a voltage of $V_{DC} - I_2(t_1) \cdot R_2$, relative to the DC- potential. The resulting voltage $V_{L12}(t)$ between the nodes can be calculated as follows.

$$V_{L12}(t_1) = -I_1(t_1) \cdot R_1 + I_2(t_1) \cdot R_2$$

The voltage $V_{L12}(t)$ increases the driving voltage across the inductor L_2 and simultaneously reduces the driving voltage across the inductor L_1. This leads to both currents converging to the value $I_{AC}(t)/2$. The course of the currents can be expressed by the following terms.

$$I_1(t) = \frac{I_{AC}(t_1)}{2} + \left[I_1(t_1) - \frac{I_{AC}(t)}{2}\right] \cdot e^{-\frac{R_1+R_2}{L_1+L_2} \cdot (t-t_1)} \qquad for: t > t_1$$

$$I_2(t) = \frac{I_{AC}(t_1)}{2} + \left[I_2(t_1) - \frac{I_{AC}(t)}{2}\right] \cdot e^{-\frac{R_1+R_2}{L_1+L_2} \cdot (t-t_1)} \qquad for: t > t_1$$

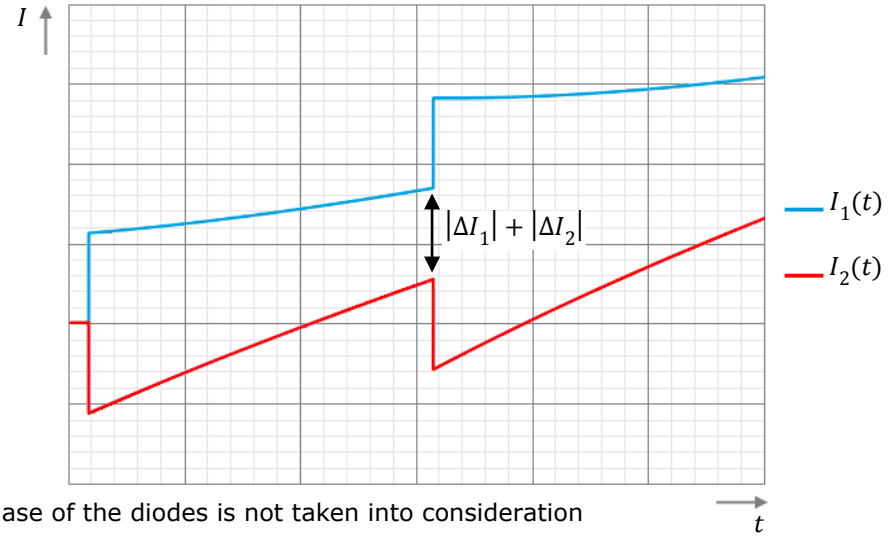
The equations show that the convergence speed of the currents $I_1(t)$ and $I_2(t)$ is determined by the ratio of the sum of the resistors R_1 and R_2 to the sum of the inductances L_1 and L_2.

$$\tau = \frac{L_1 + L_2}{R_1 + R_2}$$

If the sum of the inductances L_1 and L_2 increases, then the time constant τ increases and the convergence speed of the currents $I_1(t)$ and $I_2(t)$ decreases. The time available for the currents $I_1(t)$ and $I_2(t)$ to approach the value $I_{AC}(t)/2$ is limited by the next switching operation of the semiconductors and thus by the clock

frequency and the instantaneous value of the current $I_{AC}(t)$. The offset still present at the time of the next switching operation $\Delta I_1(t_n + x)$ or $\Delta I_2(t_n - x)$ is added to the asymmetric current distribution described in Chapter 6.2.

Figure 16: Current offset at the end of the IGBT conduction period



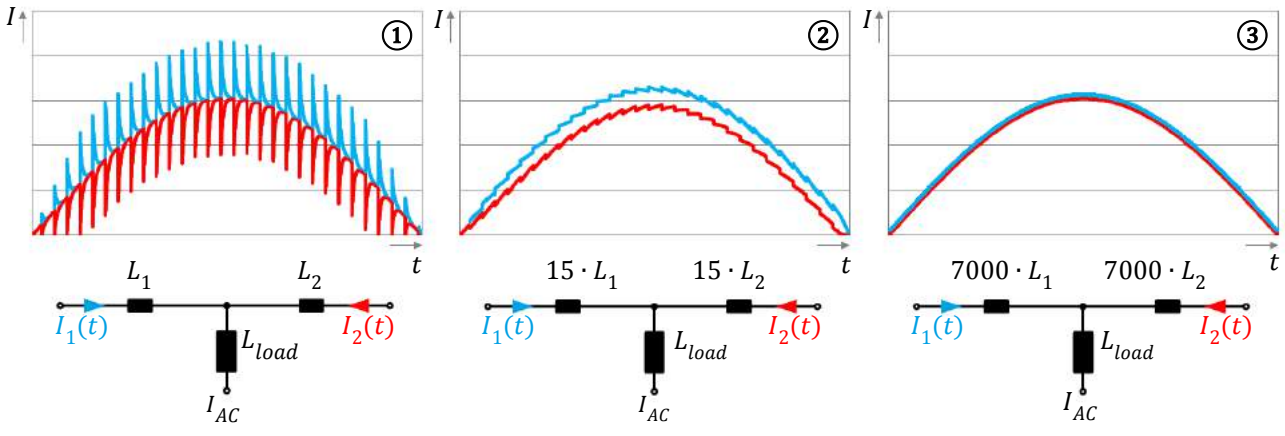
Conduction phase of the diodes is not taken into consideration

The effect of the current sharing is superimposed by the effects of the asymmetrical static current distribution, described in chapter 6.1, which works against the convergence of the currents.

6.4 Current distribution with inverter operation

In a real application, the interaction between the current distribution during the commutation phase and the common conduction phase of the semiconductors must be considered. The diagrams shown in Figure 17 apply to the parallel connection of two modules with identical characteristics in a symmetrically designed system. The effects from chapter 6.1, which describe the influence of the mechanical design on the static current distribution, are neglected. Only the results of the effects from chapter 6.2 (dynamic current distribution) and 6.3 (current sharing effect) are considered, based on different inductance values between the module outputs. The values of the inductances for case ① correspond to the parallel connection of the modules by means of a copper busbar. The values for case ② correspond to the parallel connection of the modules with power cables, and the values for case ③ correspond to the parallel connection of the modules via chokes. As a cause of the current asymmetry, a time-displacement of the drive pulses to module 1 is used, so that it turns on approximately 150ns earlier (blue trace).

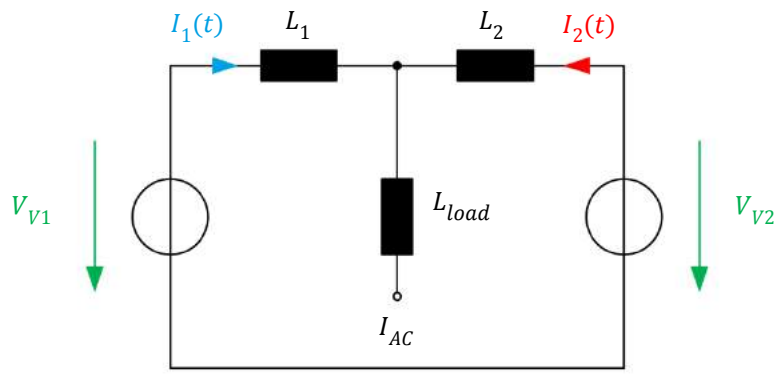
Figure 17: Influence of the AC inductance between parallel modules



The inductances L_1 and L_2 limit the slew rate of the currents $I_{AC1}(t)$ und $I_{AC2}(t)$ during the time-shifted switching of the modules. The smaller the sum of the inductance values is, the greater is the resulting

asymmetrical current distribution at the end of the commutation processes and the greater the uneven distribution of the switching losses on the modules (case ①).
The distribution of the conduction losses depends on the convergence rate of the currents. The greater the sum of the inductances L_1 and L_2 the greater the difference between the currents $I_{AC1}(t)$ and $I_{AC2}(t)$ relative to half the load current at the end of the common conduction phase of the semiconductors. The respective difference adds up over the sum of the switching operations, resulting in an unequal distribution of the conduction and switching losses of the modules (case ②).
If the values of the inductances L_1 and L_2 are rose to such an extent that a divergence of the currents $I_1(t)$ and $I_2(t)$ is minimised during the time-shifted switching processes of the modules, an almost homogeneous current distribution can be achieved (case ③). In this case, the individual modules can be considered as voltage sources. Figure 18 shows the simplified equivalent circuit diagram for two parallel modules for large AC inductances.

Figure 18: Simplified equivalent circuit diagram for two parallel modules for large AC inductors



The difference between the output voltages V_{V1} and V_{V2} is dependent on the switching time differences Δt, the switching frequency f_{sw} and the DC-bus voltage U_{DC}. The difference can be determined by the following formula.

$$V_{V1} - V_{V2} = \Delta t \cdot f_{sw} \cdot V_{DC}$$

The occurring voltage difference $V_{V1} - V_{V2}$ drives a compensation current ΔI through the inductances L_1 and L_2. The compensating current ΔI is superimposed with output currents $I_1(t)$ and $I_2(t)$. The output current is limited by the inductances L_1 and L_2.

$$\Delta I = \frac{V_{V1} - V_{V2}}{2 \cdot \pi \cdot f_{out} \cdot (L_1 + L_2)}$$

The ohmic resistances of the current branches were not taken into account for these considerations.

7. Influence of Driver Concepts on the Power Distribution

Just like the impedances of a system, the characteristics of the drivers also influence the current distribution. In contrast to the mechanical design, which mainly affects the static current distribution, the driver characteristics predominantly affect the dynamic current sharing. The reasons for this are, on the one hand, the differences in the signal propagation times and the gate-emitter voltages, as well as the influence of the jitter. On the other hand, the common emitter path, of the central driver unit, affects the current sharing.

For the following measurements, the experimental setup was constructed as symmetrically as possible in order to minimise its effects. The theoretical considerations assume that the semiconductors or modules connected in parallel have identical characteristics.

7.1 Influence of the individual drivers on the dynamic current distribution

7.1.1 Differences in signal propagation times

The signal propagation time is defined by the time of a valid change of state of the signal at the input of an electronic module, up until a valid change of state of the corresponding output signal. The more devices a signal has to pass, the higher the probability that the differences between the sums of the signal propagation times increase. The likelihood that the output signals of parallel assemblies will change state at the same time decreases with the number of devices that the signals pass.

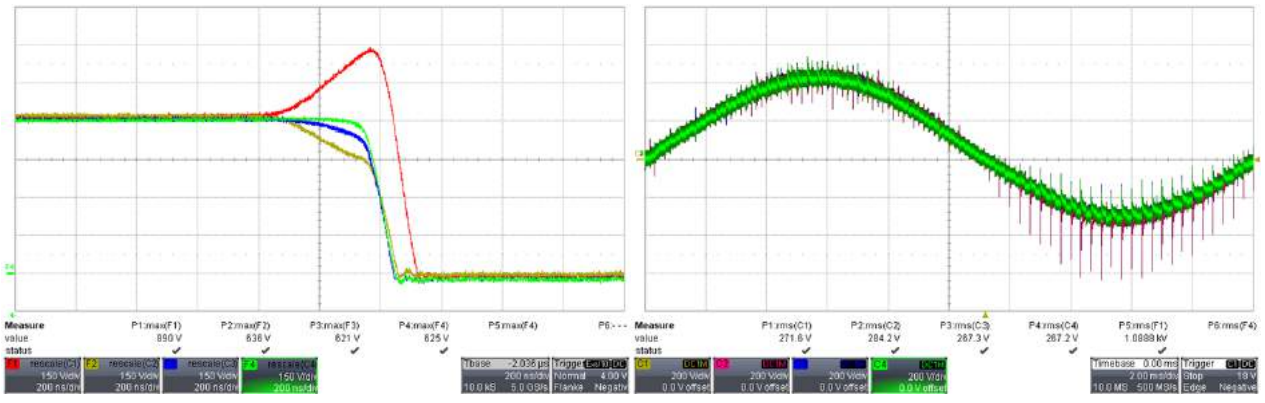
$$\Delta t_p = \sum_{i=1}^{n} \left(t_{p1,i} - t_{p2,i} \right)$$

With regard to the driver concepts, this means that only a small difference between the signal propagation times is much more probable when a central driver is used than in the case of the parallel connection of individual drivers.

The left diagram in Figure 19 shows the measurement results of IGBT current of the pulse test for the parallel SEMIX603GB12Ep modules. Each of the modules was controlled by a dedicated SKYPER12 press-fit driver. One of the drivers was prepared in such a way that the associated IGBT (red trace) switches off with a delay time of approx. 100ns. Due to the longer conduction phase of the IGBT, the currents of the parallel IGBTs do not immediately commutate to the corresponding freewheel diodes, but partly flow through the still conducting IGBT. In this test arrangement, a current increase of approx. 48% occurs, based on the nominal value $I_{C,sum}/4$. The distribution of the currents, during the commutation sequences of the IGBTs, takes place according to the concept described in chapter 6.2.

The results for the inverter operation can be found in the right diagram in Figure 19, in which one of the BOT IGBTs (red trace) is switched on approximately 100ns earlier.
The real time offset between parallel SKYPER12 press-fit drivers, which occurs due to the signal propagation time tolerances, is significantly less than 100ns. The influence of the switching under realistic delay times can be seen on the positive half-wave of the right diagram.

Figure 19: Measurement of the influence of different signal propagation times



IGBT turn off; collector current; 150A/div; 200ns/div

inverter mode; AC current; 200A/div; 2ms/div

7.1.2 Jitter

The influence of the jitter occurs with digital drivers connected in parallel, when they have their own system clock. The maximum time offset due to jitter is determined by the frequency of the system clock. If the input signal changes simultaneously at the parallel driver stages, the change in the corresponding output signal may vary in time by the length of one system clock period.

$$t_{jitter,max} = \frac{1}{f_{clock}}$$

The time offset variance due to jitter approximately shows a Gaussian normal distribution over the values $0 \leq t_{jitter} \leq T_{clock}$. It is therefore not foreseeable which driver provides a valid output signal at which time. Looking at the effect of the jitter in isolation, it can be assumed that with an increasing number of signal changes at the input of the parallel drivers, the summed time offset variance between the output signals approaches zero.

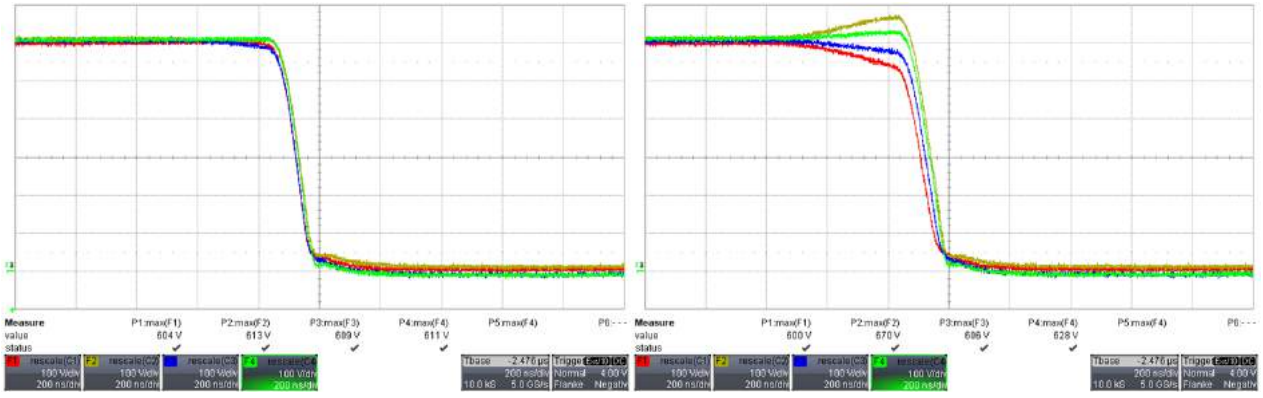
$$\sum_{i=1}^{n} t_{jitter,i} - \sum_{k=1}^{n} t_{jitter,k} \approx 0 \qquad for: n \to \infty$$

In the real application, the time offset of the jitter is added to the time offset of the different signal propagation times. The effect of the jitter can, however, be neglected for the central driver concept.

$$t_d = \Delta t_p + t_{jitter}$$

Figure 20 shows the measured results of the pulse test with four parallel individual drivers. The delay time due to the jitter is approximately 25ns, which corresponds to the reciprocal of the system frequency of the SKYPER12 press-fit driver of 40Mhz. The measured values of both diagrams were recorded under identical conditions and in immediate succession. The left diagram shows a nearly symmetrical current distribution. The delay between the driver outputs is almost zero at this time. The right diagram shows the effect on the dynamic current distribution with a time delay of approx. 25ns between the outputs of the parallel drivers. In this measurement, a time delay of approx. 25ns results in a current increase of approx. 12% (yellow trace), based on the nominal value $I_{C,sum}/4$. The currents distribute according to the concept described in chapter 6.2.

Figure 20: Measurement of the influence of the jitter



IGBT turn off; collector current; 100A/div; 200ns/div

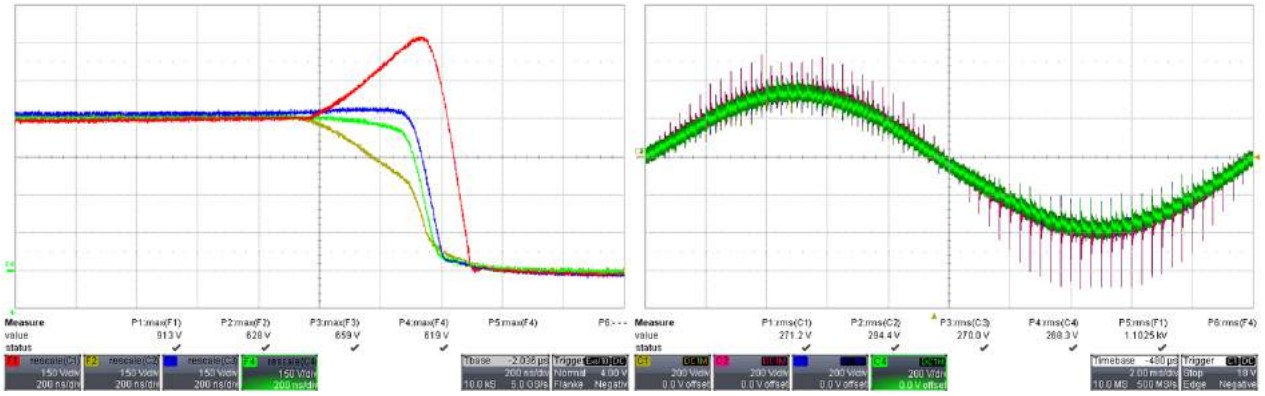
IGBT turn off; collector current; 100A/div; 200ns/div

7.1.3 Differences in gate-emitter voltages

It can be assumed approximately that the switching speed of an IGBT depends on the speed of the charging and discharging of its input capacitance. On the presumption that the parallel-connected semiconductors have identical characteristics and the gate circuits are identical, the gate-emitter voltage determined by the driver sets the speed of the charging process.
If each semiconductor module has an individual driver with its own gate voltage regulation, differences in the gate-emitter voltages between the modules may occur. This can be neglected for the central driver concept.
To illustrate this effect, the gate turn-on and gate turn-off voltage of a driver (red trace) was increased by approximately 0.7V. As a result, the corresponding IGBT turns on faster and turns off slower.
The left diagram in Figure 21 shows the dynamic current distribution during a turn-off process. Due to the longer conduction phase of the IGBT, the currents of the parallel IGBTs do not immediately commutate to the corresponding freewheel diodes, but partly flow through the still conducting IGBT. During this particular

switching process, there is a current increase of approx. 52%, based on the nominal value $I_{C,sum}/4$. The distribution of the currents, during the commutation processes of the IGBTs, takes place according to the concept described in chapter 6.2.
The right diagram shows the measured results for the inverter test. Here too, the time-delayed switching can be seen clearly displayed by the current peaks of the red trace. This affects the total current distribution with a deviation of approx. 7% from the nominal value $I_{AC}/4$.

Figure 21: Measurement of the influence of different gate-emitter voltages



IGBT turn off; collector current; 150A/div; 200ns/div

inverter mode; AC current; 200A/div; 2ms/div

7.2 Influence of the central driver on the dynamic current distribution

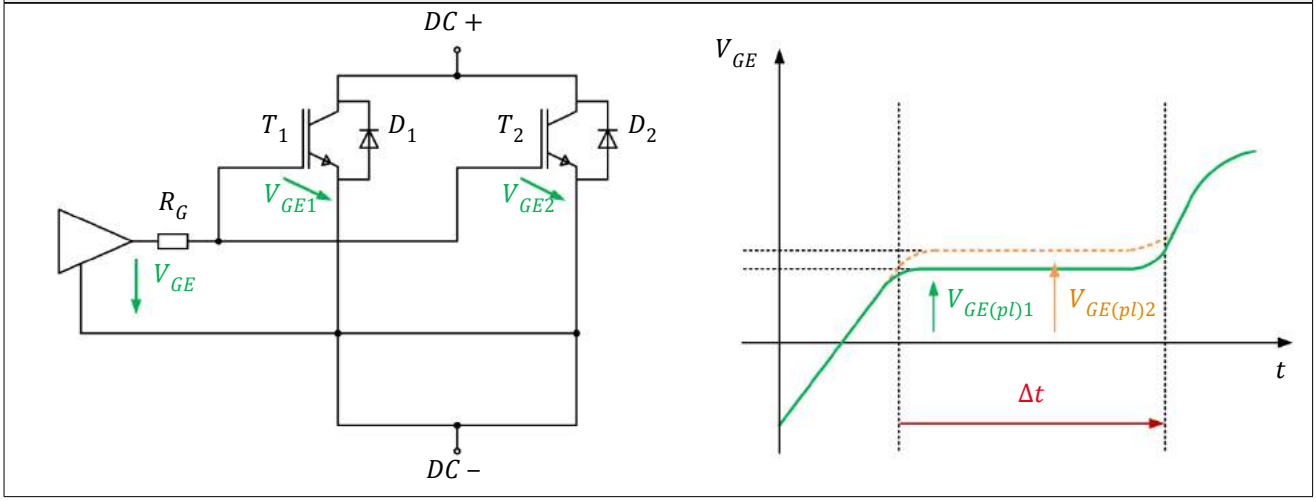
With a central driver all parallel IGBT modules are controlled by this one driver. In order to ensure a good current distribution, a few points have to be considered.

7.2.1 Gate resistor

In the case of direct parallel connection of the IGBT gates from a central driver, the IGBT (T_1) with the steeper transfer characteristic clamps the gate voltage of the parallel IGBT (T_2) on the level of its plateau voltage $V_{GE(pl)1}$. IGBT T_1 takes up more current as long as it clamps the gate voltage (Δt). When the inverse diodes take full blocking voltage the gate voltage increases again and both IGBTs could turn on fully.

In order to avoid this, a separate gate resistor is provided for each IGBT. The gate voltage on the IGBTs can then rise independently of one another, which results in only slight switching differences.

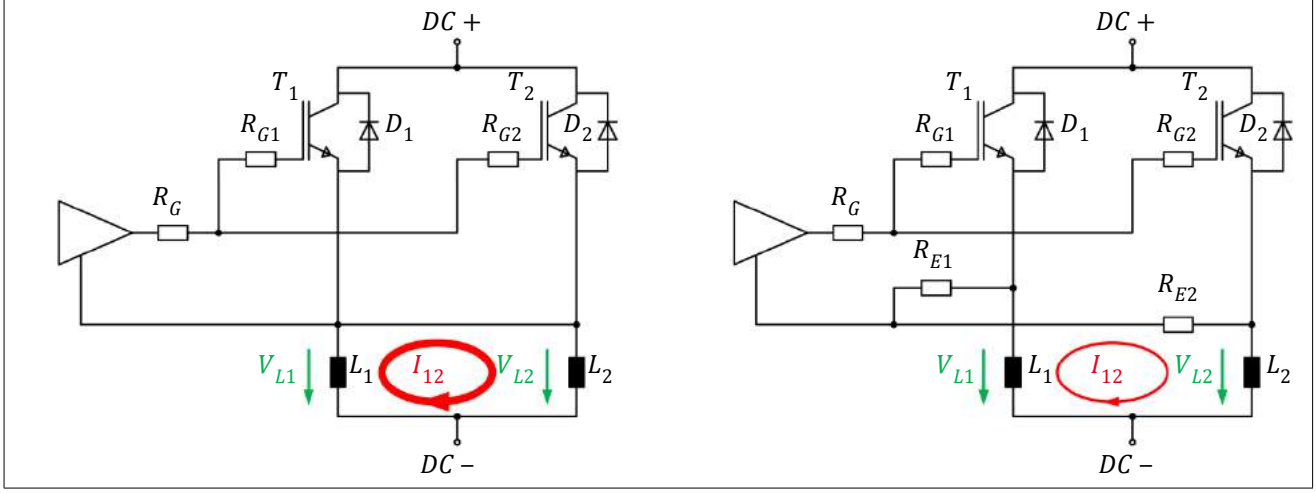
Figure 22: Equivalent circuit diagram for two parallel IGBTs without individual gate resistors



7.2.2 Emitter resistor

Figure 23 shows one the left side a hard emitter connection of the driver to the IGBTs and the stray inductances in the emitter connection. For the TOP IGBTs, the stray inductance results from the AC connection of the modules. For the BOT IGBTs this is the inductance in the DC minus connection. Different switching speeds of the IGBTs or different inductances result in different voltage drops V_{L1} and V_{L2}. These different voltage drops cause a circulating current I_{12} flowing through the emitter connection of the driver. This circulating current can reach high values and overload the thin auxiliary emitter terminals.
To avoid this, current-limiting resistors are inserted into the emitter connections of the driver. With balanced emitter inductances good results have been achieved with an emitter resistance of $R_E = 0{,}5\Omega$. Note that this resistor is in series with the gate resistance and therefore has an influence on the switching behaviour of the IGBT.

Figure 23: Equivalent circuit diagram for hard common emitter connection (left) and common emitter connection with emitter resistors (right)



7.2.3 Emitter feedback

When controlling the IGBTs via a central driver, the coupling of the gates via the common emitter has a balancing effect. This is an advantage over the solution with individual drivers where the currents can vary independently of each other. This balancing effect is explained by the example of two IGBTs connected in parallel, Figure 24.

If IGBT T_1 switches earlier than T_2, a voltage drop occurs at the emitter inductance L_1. This voltage drop leads to a current (I_{12}, blue line) through the emitter resistors R_{E1} and R_{E2}. The current causes a voltage drop at the emitter resistors which counteracts the gate voltage at T_1 and adds to the gate voltage at T_2.

$$V_{GE1} = V_{GE} - V_{RG1} - V_{RE1}$$

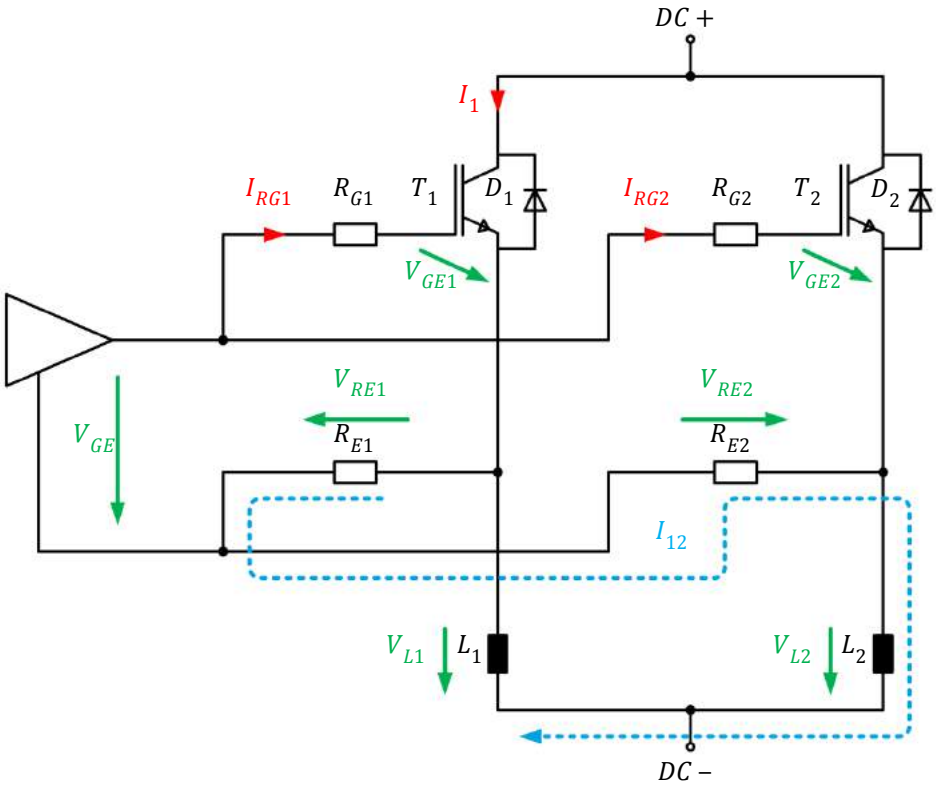
$$V_{GE2} = V_{GE} - V_{RG2} + V_{RE2}$$

This means that the gate voltage is reduced on the IGBT which switches first (T_1), causing this to be delayed. This effect is referred to as negative feedback. On the IGBT which switches later (T_2), the gate voltage increases, whereby this switches faster (positive feedback). This means that the currents are balanced during switching.

However, this balancing due to the emitter coupling has limitations:

- When the emitter inductance is large, the coupling becomes too strong. Even slight differences in the switching speed of the parallel IGBTs result in high gate voltage differences, which can lead to oscillations.
- For unbalanced emitter inductances (for example, $L_1 \gg L_2$), and even if the IGBTs have the same switching characteristics, different couplings to the gate voltages occur, resulting in different switching.

Figure 24: Equivalent circuit diagram with two parallel IGBTs with common emitter

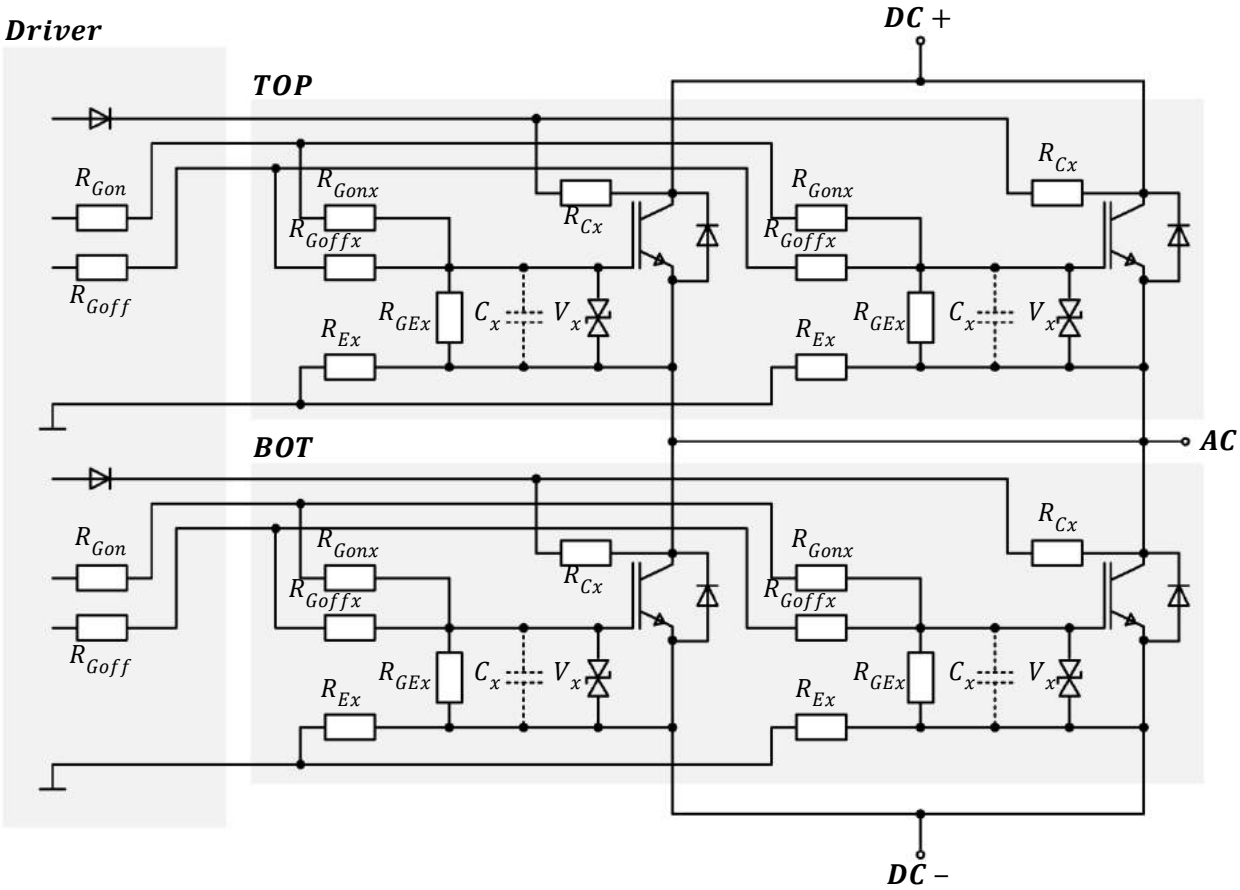


For this reason, in the design low and symmetrical emitter inductances are a must. This is more critical with the TOP switch than with the BOT switch because the AC connection usually has a higher inductance than the minus of the DC-bus.
This also shows the limits for a central driver. For systems with higher power, many modules must be connected in parallel so that the emitter connections become longer and thus the emitter inductance is large and unbalanced. As described, this leads to uneven current distribution and oscillations. This is why individual drivers are used for large systems.

7.3 Additional gate drive components

In addition to the gate (R_{Gx}) and emitter resistors (R_{Ex}), a resistor (R_{GEx}) should be connected gate to emitter. This is to prevent the IGBTs from inadvertently turning on when the driver is not supplied. The resistance usually has a value of 10kOhm.
To protect the gate from overvoltage, Zener diodes (V_{x}) or suppressor diodes are connected from gate to emitter. Make sure that the threshold of the diode is above the maximum gate voltage of the driver but below the maximum allowed gate voltage of the IGBT (+/-20V).
Possibly a capacitor (C_{x}) parallel to gate and emitter may have a positive effect on the parallel operation. The capacitor is in the range 10% ... 50% of the IGBT gate-emitter capacity. The effect can be tested in the double pulse test.
If overcurrent and short circuit protection is implemented on the basis of V_{CEsat} evaluation, a resistor (R_{Cx}) is used to determine the actual value for V_{CE}.
The resistors and protective circuitry must be close to the module. For this purpose an interface board should be developed which contains these components. For this interface board, ensure identical cable length to the parallel IGBTs. Gate and emitter tracks are to be run in parallel.
The driver core can then be plugged directly onto the interface board or connected via cables. The wires should be twisted-pair.

Figure 25: Block diagram of two parallel-connected modules with interface board and driver



8. Summary

In order to minimise the influence of the semiconductor properties on the current distribution, modules from one batch should be used. In general, a current unbalance of 5% should be expected. This current asymmetry must be taken into account when calculating the conduction and the switching losses.

In order to achieve a symmetrical current distribution it is important to ensure that the impedances of the parallel current paths are as equal as possible. To ensure this, the AC connection should be routed centrally to the parallel-connected modules with the same length to the individual modules. The load cable should be routed at a distance from the modules so that the inductance of the modules to the load stays as balanced as possible.

In the inverter test, the current distribution is significantly better than in the double pulse test due to the positive IGBT temperature coefficient and the high load inductance. The double pulse test is well suited for investigating the switching behaviour and the symmetry but not the current distribution of parallel connected modules.

When selecting the driver concept, the size of the system is crucial. For compact systems, a solution with a central driver is preferable. The negative influences on the current distribution caused by the jitter, the differences in the signal propagation times, as well as the differences in the gate-emitter voltages are largely done away with in this concept. In addition, there is the positive effect of emitter feedback.

In the case of larger systems, the shared emitter path increases by design, and oscillations between the parallel semiconductors or modules can occur due to the emitter feedback. In this case, the concept with individual drivers must be used.

If individual drivers are used, care must be taken that the differences between the signal propagation times of the drivers and the time differences due to the jitter are as low as possible. The time lag between the drive signals of the IGBTs and the differences in the switching speeds of the IGBTs themselves are critical when dimensioning the AC inductances. With low jitter and low differences in the signal propagation times, an additional AC inductor is generally not required and the modules can be connected hard parallel.
If the current asymmetry of a hard parallel circuit is higher than the desired value, the parallel current branches must be decoupled via as large inductances as possible. Particularly separate motor or line filter windings are suitable for this because, in the case of high power, they are frequently already composed of parallel-connected winding systems.

Symbols and Terms

Letter Symbol	Term
ΔI	Delta of current
Δt	Delta of time
C	Capacitor
D	Diode
DC+	Positive DC-Link voltage
DC-	Negative DC-Link voltage
di/dt	Change of current per time
f_{clock}	Internal clock frequency
f_{out}	Output frequency
f_{sw}	Switching frequency
g_{fs}	Forward tansconductance
I	Current
I_{AC}	Output current
$I_{AC,sum}$	Total output current

Letter Symbol	Term
I_C	Continuous collector current
$I_{C,sum}$	Total continuous collector current
i_C	Collector current
i_F	Forward current (actual value)
IGBT	Isolated gate bipolar transistor
K	Branch point
L	Inductance
L_σ	Stray inductance
$L_{\sigma E}$	Emitter stray inductance
$L_{\sigma G}$	Gate stray inductance
L_{load}	Load inductance
M	Magnetic coupling
NTC	Negative temperature coefficient
PTC	Positive temperature coefficient
r_{CE}	On-state slope resistance
R	Resistor
R_E	Emitter circuit resistance
R_G	Gate circuit resistance
τ	Tau
t	Time
T	IGBT / temperature
T_{clock}	Cycle duration of internal clock frequency
t_d	Delay time
T_j	Junction temperature
t_{jitter}	Jitter
t_p	Propagation delay time
T_{sense}	Sensor temperature (module)
V	Voltage
V_{CE}	Collector-emitter voltage
V_{CEsat}	Collector-emitter saturation voltage
V_{DC}	DC-voltage
V_F	Forward voltage

Letter Symbol	Term
$V_{G(off)}$	Turn-off gate voltage level (driver)
$V_{G(on)}$	Turn-on gate voltage level (driver)
V_{GE}	Gate-emitter voltage
$V_{GE(pl)}$	Gate-emitter plateau voltage
$V_{GE(th)}$	Gate-emitter threshold voltage

A detailed explanation of the terms and symbols can be found in the "Application Manual Power Semiconductors" [2]

References

[1] www.SEMIKRON.com
[2] A. Wintrich, U. Nicolai, W. Tursky, T. Reimann, "Application Manual Power Semiconductors", 2nd edition, ISLE Verlag 2015, ISBN 978-3-938843-83-3
[3] M. Spang, "Current sharing between parallel IGBTs in power modules during short circuit with unsymmetrically connected load", 2016

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