Comparison of 3-Level Topologies NPC and ANPC under the Aspect of Low Voltage Ride Through, SiC and Energy Storage Capability

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Abstract

Recently, renewable energy has become increasingly important and the share of solar energy in particular has risen sharply. The increasing connection of alternative energy sources to the low or medium voltage grid requires new regulations.
In [1] 10 trends in the solar sector up to 2025 were compiled, from which potential requirements for power electronics and module manufacturers can be derived.
This paper considers 3-Level topologies from the point of view of some of these requirements and potential trends. These include:

- the increasing requirements regarding reduced harmonic content and Low Voltage Ride Through (LVRT)
- the potentially higher usage of wide bandgap semiconductors
- the energy storage capability and the associated extended power factor range

1. Introduction

3-Level topologies are state of the art and are widely used in solar applications. The most commonly used variants include the TNPC, NPC and ANPC. While the TNPC is used in applications up to a maximum DC bus voltage of $1000V_{DC}$, the NPC and ANPC are mainly used in voltage ranges up to $1500V_{DC}$.
The trend towards energy storage capability also requires an extended power factor (pf) range.
While today's solar inverters operate in a nominal power factor range of pf=0.8...1, charging and discharging the battery requires an additional power factor at pf=-1. This results in increased requirements for the diode area within the power modules.
The Low Voltage Ride Through (LVRT) requirement is another factor influencing the diode area.
With the extended power factor range, LVRT requirement and use of SiC semiconductors, the NPC and ANPC are evaluated. The latter in execution of two different control procedures.

2. Low Voltage Ride Through

The expansion of renewable energies has increased continuously in recent years. For the connection of a generation unit to the public grid, both stationary and dynamic requirements must be met in the event of a grid fault. In Germany, the BDEW Medium Voltage Directive [2] and the Transmission Code [3] are the technical basis for this. If a grid fault occurs, the inverter must remain connected to the grid, be able to pass through it and feed in a defined reactive current. This property is called Fault Ride Through. A special case is the voltage dip which is called Low Voltage Ride Through. In this case the inverter must feed in a capacitive reactive current in order to increase the voltage.
The inverter must meet the requirements of a specific grid code. Fig. 1 shows the LVRT requirements for different country-specific grid codes as a voltage curve over time.

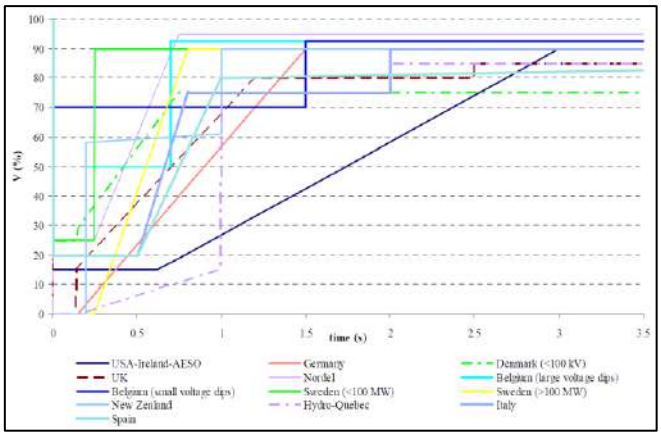


Fig. 1. LVRT requirements of various grid codes [4]

Fig. 2 shows an example from the German grid code, which shows the voltage drop an inverter must pass through in case of a grid fault without disconnecting from the grid.

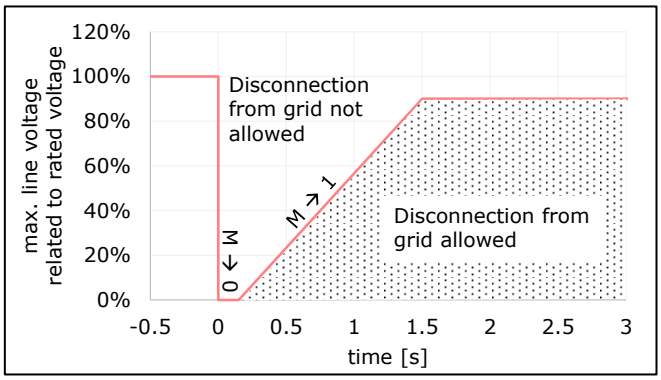


Fig. 2. German LVRT grid code [5]

The grid line voltage drops to 0% of the rated voltage at the time of the fault, stays for 0.15s at low level and rises to 90% at 1.5s after the error occurs. If the grid voltage remains at a low level for a longer period of time, the voltage curve leaves the range shown here and the inverter can disconnect from the grid. The modulation index M of the inverter follows the mains voltage. This means that when the voltage drops, M approaches zero and rises again in the direction of M=1 up to 1.5s after the voltage drops.
In [6] different operating modes of solar inverters are described. The operating mode Fault Ride Through "Full" described in it illustrates the requirements based on a voltage drop to 5% of the nominal grid voltage.
Fig. 3 shows a 3-phase voltage curve with a drop to 5% of the nominal grid voltage and the current curve.

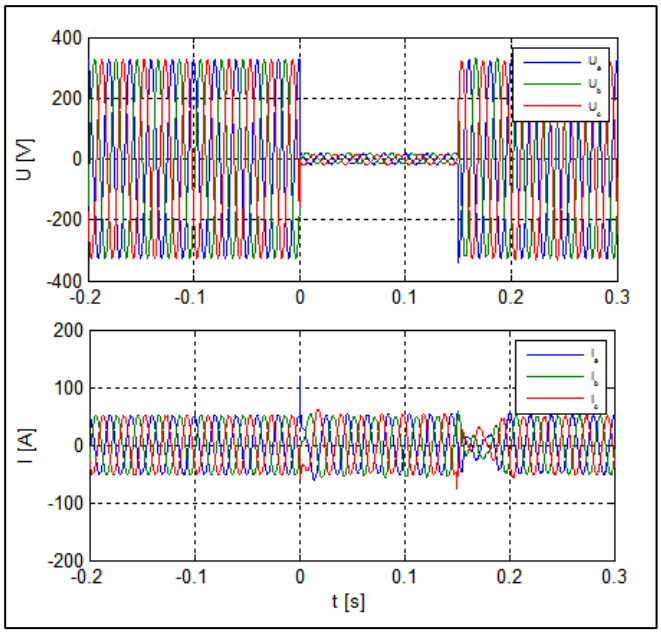


Fig. 3. Real response to a 5% Vn voltage dip by the PV inverter STP 25000TL-30 in the FRT “full” operating mode [6]

This operating mode requires that the inverter remains connected to the grid and feeds reactive current according to e.g. one of the LVRT requirements shown in Fig. 1.
The resulting requirements on the inverter (pf=0, low modulation index M → 0) place special demands on the different switches of the NPC and the ANPC topologies. Appropriate chip sizes must be selected when designing the power modules to meet these LVRT requirements, especially when considering SiC devices.

3. 3-Level topologies NPC, ANPC HF/LF and ANPC LF/HF

The PWM strategies of the NPC and ANPC are sufficiently described in the reference material. For the NPC the control procedure according to [7] is considered. For the ANPC, the control procedures described as PWM-1 (ANPC HF/LF) and PWM-2 (ANPC LF/HF) are considered [8], [9], which differ in the control of the input and output stage. HF stands for high frequency and LF for low frequency. Fig. 4 compares the three topologies. The red and blue dotted paths represent the respective commutation paths for positive and negative output current at pf=1 and pf=-1.
The focus is only on those switches that switch with a switching frequency f_{sw} in the kilohertz f_{kHz} range. The commutation of the remaining

switches, which occurs only once per output period f_{out} (e.g. 50/60Hz), can be neglected as switching event, since the switching losses P_{sw} that occur in this case do not contribute significantly to the total losses.
The NPC has the same commutation path as the ANPC HF/LF at pf=1. If pf=-1, the commutation path is the same as the ANPC LF/HF. The commutation paths of the ANPC HF/LF are always small and the ANPC LF/HF are always long regardless of the power factor.

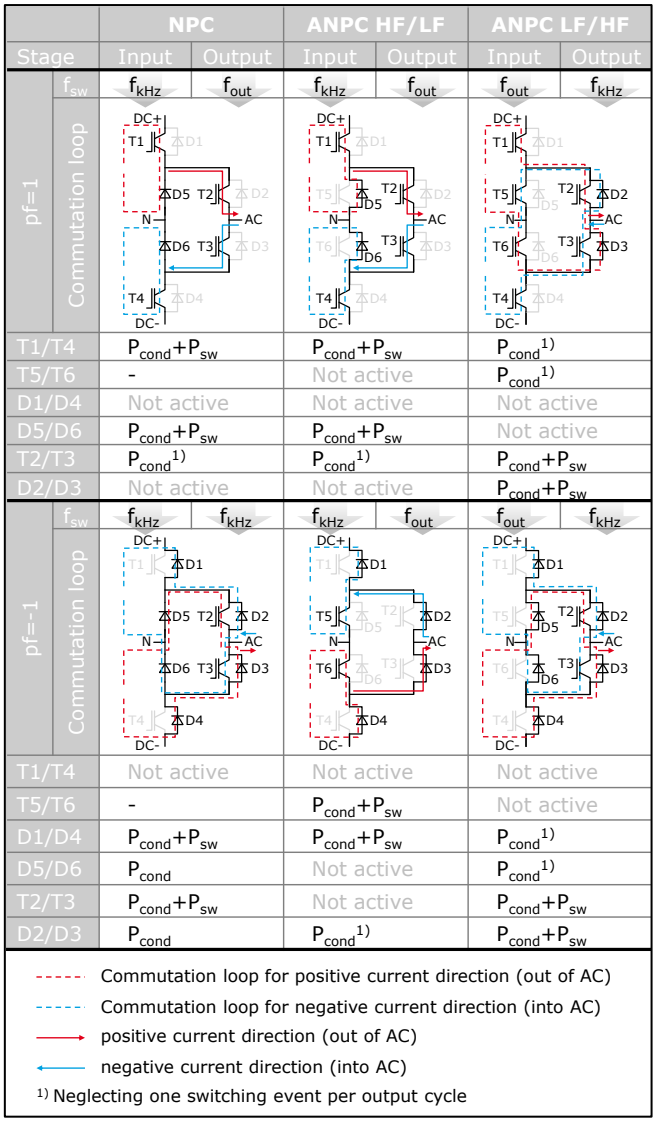


Fig. 4. Commutation paths of NPC, ANPC HF/LF, ANPC LF/HF at pf=1/-1, positive/negative current direction

4. Use of Silicon Carbide Devices

The use of Silicon Carbide (SiC) components is intended for those switches where high switching losses occur. In contrast to their Si counterparts, SiC Schottky Barrier diodes (SiC-SBD) have no reverse recovery charge. This characteristic significantly reduces the switching losses of the SiC-SBD to 2...3% compared to a corresponding Si diode. The switching losses can be neglected for this reason. In addition, the turn-on losses of the corresponding IGBT are reduced down to approx. 40% compared to a Si-diode.
Based on the type of power dissipation according to Fig. 4, the diode positions relevant for SiC-SBD can be determined, which are marked in red in Fig. 5.

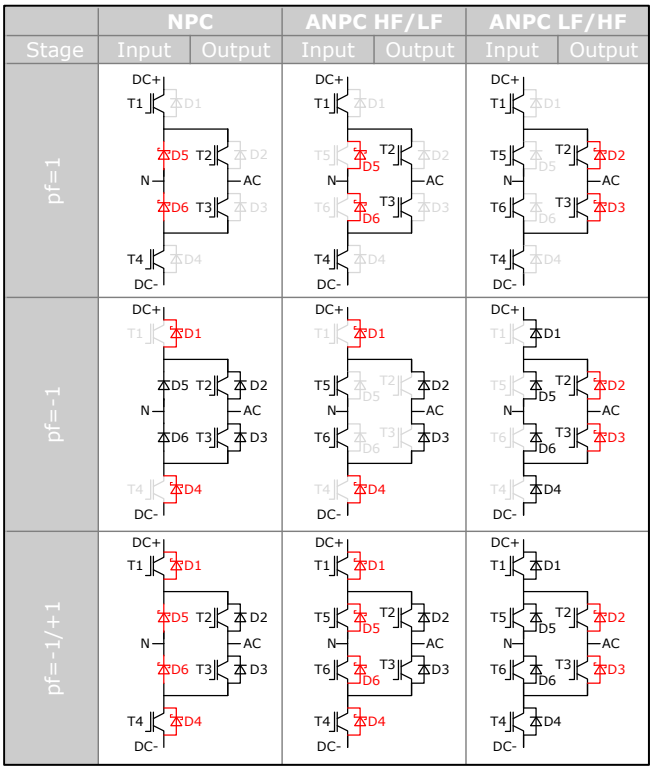


Fig. 5. Relevant positions for the use of SiC-SBD

The use of SiC-SBD at the respective positions depends on the power factor for the NPC and ANPC HF/LF. The ANPC LF/HF, on the other hand, only benefits from SiC-SBD at positions D2/D3, which are active over the entire power factor range for all M>0. While the NPC and ANPC HF/LF must be equipped with SiC-SBD at up to four chip positions, two positions are sufficient for the ANPC LF/HF.

To further reduce switching losses or to use higher switching frequencies, SiC-MOSFETs can be used instead of IGBTs. In combination with SiC-SBD they additionally increase the efficiency.

5. 62mm Half-bridge Power Modules

Standard 62mm half-bridge modules are considered for the implementation of 3-Level topologies. These are characterized by a low module stray inductance and low prices. Fig. 6 shows different standard topologies in the respective package. As an example, in IGBT4 technology single switches are available up to 900A/1200V, half-bridge and Buck/Boost modules up to 600A/1200V.

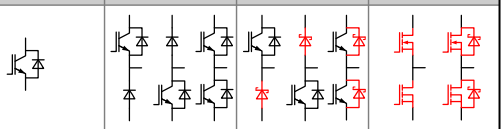
	Single switch	Buck / Boost / Half-bridge			
1200V	Full-Si	Full-Si	Hybrid Si+SiC	Full-SiC	
topology					
Power module					
200A		x	x		
300A	x	x			
350A				x	x
400A	x	x			
450A		x			
500A				x	
600A	x	x			
900A	x				

Fig. 6. Standard 62mm half-bridge modules with different chip options

The NPC and ANPC can be assembled from these standard modules. Fig. 7 shows two different options for all three topologies. For a "Low Output Power" application without parallel connection three standard modules are used. The NPC is composed of three different modules; the ANPC topologies of only two. For higher power, several modules can be connected in parallel. For the output stage of the ANPC HF/LF as well as the input stage of the ANPC LF/HF single switches can be considered, which are available up to a current rating of 900A. Although the maximum output current is limited by the input stage on the ANPC HF/LF and by the output stage on the ANPC LF/HF, single switches with a high current rating offer the option to increase efficiency at a given output current. To reduce the harmonic content of the output current, the output stages of the ANPC LF/HF can be interleaved. This reduces the current ripple at a given switching frequency according to the number of interleaved output stages.

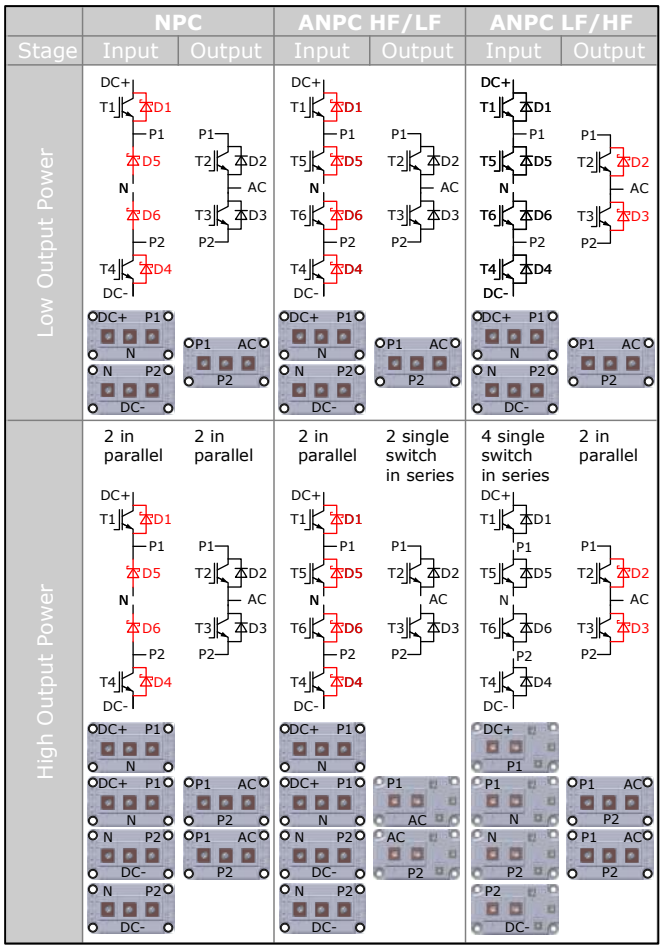


Fig. 7. Module options for different output power

6. Overvoltage protection

As shown in Fig. 4, different commutation paths apply to all three considered topologies. The ANPC HF/LF has the advantage that the high-frequency commutation always takes place within a half-bridge module. The ANPC LF/HF on the other hand always has a long commutation path including three modules. The NPC only has a small commutation path identical to the ANPC HF/LF at pf=1. As soon as the power factor moves away from 1, also the long commutation paths across three modules come into operation.

The commutation paths require measures for overvoltage limitation of the power semiconductors depending on

- the maximum DC-Link voltage,
- the maximum current to be switched and
- the choice of gate resistors.

The advantage of the 62mm module is to allow a low-inductance DC-Link consisting of a laminated bus bar. Thus all three DC potentials (DC+, DC-, N) can overlap extensively to keep the DC-Link inductance low.
For the NPC and ANPC HF/LF a normal C-snubber can be provided at the DC terminals of both modules of the input stage. In the case of the NPC, due to the control method under consideration, a C-snubber cannot be used for the output stage because T2 and T3 can conduct simultaneously. In this case, an RC- or RCD-snubber would need to be provided. An alternative would be a software solution that prevents an overvoltage in the switching moment by slowing down the turn-off times. However, this would increase the switching losses.
For the ANPC LF/HF only a C-snubber across the output stage is required. The gate-emitter connectors of the input stage are screw contacts and can be connected to the driver via cable.
As an example for High Output Power, Fig. 8 shows the three topologies regarding the use of snubbers as well as notches in the bus bar for the gate-emitter connectors.

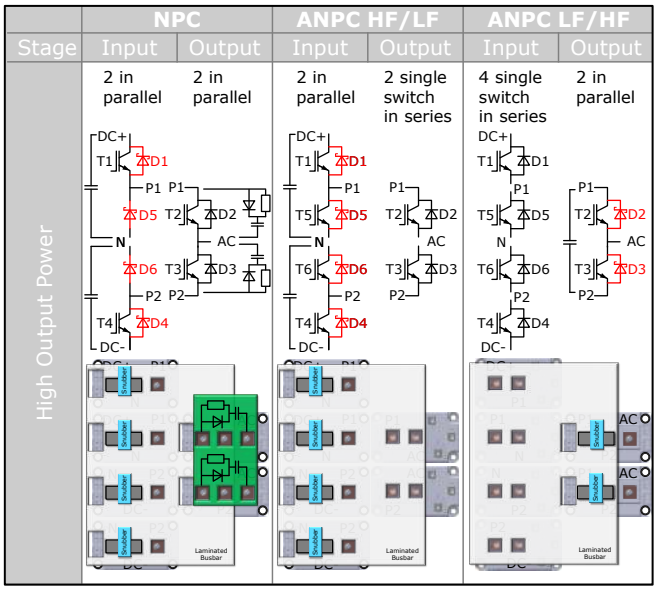


Fig. 8. Use of snubbers and simplified bus bar design

7. Performance comparison

When comparing the current load of the individual diodes, only those positions where SiC-SBD are used are considered. Furthermore, switching losses are neglected. The conduction losses P_{cond} can be calculated for the diode as follows:

$$P_{cond}(T_j) = V_{F0}(T_j)\frac{1}{T}\int_0^T i(t)dt + r_F(T_j)\frac{1}{T}\int_0^T i^2(t)dt$$

With the definition of the average and the square RMS current:

$$I_{avg} = \frac{1}{T}\int_0^T i(t)dt$$

$$I_{rms}^2 = \frac{1}{T}\int_0^T i^2(t)dt$$

the formula for the conduction losses can be written as:

$$P_{cond}(T_j) = V_{F0}(T_j)I_{avg} + r_F(T_j)I_{rms}^2$$

$V_{F0}(T_j)$ – junction temperature (T_j) – dependent threshold voltage of the on-state characteristic
$r_F(T_j)$ – junction temperature (T_j) – dependent bulk resistance of the on-state characteristic

Assuming SiC-SBD with identical values for V_{F0} and r_F, an evaluation of the conduction losses for the individual chip positions can be performed using the quantities I_{avg} and I_{rms}. The statement about the required SiC-SBD area is made under the aspect of an identical junction temperature T_j of the diodes. However, this is the ideal case, since only certain chip sizes are available.

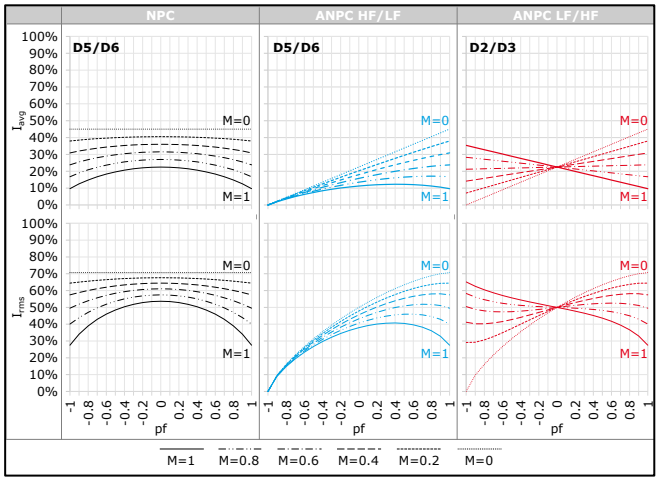


Fig. 9. I_{avg} and I_{rms} current for D5/D6 (NPC, ANPC HF/LF) and D2/D3 (ANPC LF/HF)

Fig. 9 shows I_{avg} and I_{rms} for D5/D6 of the NPC and ANPC HF/LF and for D2/D3 of the ANPC LF/HF. The percentage refers to the RMS value of the output current.
Fig. 10 shows I_{avg} and I_{rms} for D1/D4 of NPC and ANPC HF/LF and for D2/D3 of ANPC LF/HF.
The depicted curves are based on the analytical expressions for the average and RMS currents given in the appendix.

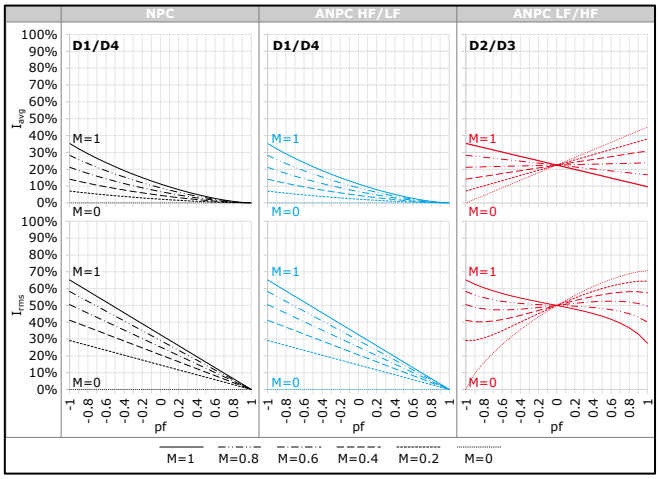


Fig. 10. I_{avg} and I_{rms} current for D1/D4 (NPC, ANPC HF/LF) and D2/D3 (ANPC LF/HF)

Depending on the required power factor, the following statements can be made:
If only inverter operation at pf=1 is required, all three topologies behave identically with respect to SiC-SBD area. At positions D1/D4 no SiC is required, i.e. two SiC-SBD are sufficient. If only high modulation indices are relevant, only little diode area is needed at all positions.
If the application additionally requires energy storage capability at pf=-1 and high modulation indices, larger SiC-SBD must be used in the NPC and ANPC HF/LF for D1/D4 each. For the ANPC LF/HF, D2/D3 must be enlarged. In this case the ANPC LF/HF has a cost advantage in terms of SiC area requirements.
If LVRT capability (pf≈0, M≈0) is required in addition to inverter operation and energy storage (pf=+/-1), the previously small area for D5/D6 must be increased for the NPC. In this case, the cost advantage of the ANPC LF/HF compared to the NPC increases further.
If the application requires only LVRT in addition to the inverter operation pf=1, but no energy storage (pf=-1), no SiC-SBD at D1/D4 are required for the NPC and ANPC HF/LF, because in the LVRT the efficiency is not decisive. In addition, the current load in D1/D4 decreases with decreasing modulation index. For both ANPC topologies the small SiC area remains sufficient, whereas for NPC large diodes D5/D6 are required.
Fig. 11 summarizes the relative sizes of the required SiC-SBD area depending on the operating mode.

	NPC	ANPC HF/LF	ANPC LF/HF
pf≈1, 0.5≤M≤1 (inverter)	D5/D6: small	D5/D6: small	D2/D3: small
pf≈1, 0.5≤M≤1 (inverter) and pf≈-1, 0.5≤M≤1 (storage)	D5/D6: small D1/D4: medium	D5/D6: small D1/D4: medium	D2/D3: medium
pf≈1, 0.5≤M≤1 (inverter) and pf≈0, M≈0 (LVRT)	D5/D6: large	D5/D6: small	D2/D3: small
pf≈1, 0.5≤M≤1 (inverter) and pf≈-1, 0.5≤M≤1 (storage) and pf≈0, M≈0 (LVRT)	D5/D6: large D1/D4: medium	D5/D6: small D1/D4: medium	D2/D3: medium

Fig. 11. Relative size of the required diode area

In order to verify the statements made based on the analytical equations, a simulation of the three mentioned operating points is carried out as a comparison. For this purpose SemiSel [10] is used as online simulation tool.
The inverter and energy storage operating points are defined in Fig. 12.

Parameter	inverter	storage
DC-Link voltage V_{dc}	1200V	
Line to line output voltage V_{ac}	690V	
Output current I_{ac}	130A	
Power factor pf	1	-1
Output frequency f_{out}	50Hz	
Switching frequency f_{sw}	12kHz	
Modulation	SVPWM	
Heatsink temperature (fixed)	80°C	

Fig. 12. Operating point inverter and energy storage mode

The modulation index M is close to 1.
The following power modules [11], [12] listed in Fig. 13 are considered. For the simulation datasheet power loss values at R_{gon}=R_{goff}=1Ω have been used.

	NPC		ANPC HF/LF		ANPC LF/HF	
Stage	Input	Output	Input	Output	Input	Output
SKM200GB12F4SiC3	x		x			x
SKM200GB12E4		x		x	x	

Fig. 13. Considered power modules for simulation

Fig. 14 shows the average conduction losses and the average junction temperature over an output period for inverter operation.

The power loss curves of the corresponding diodes are identical. This corresponds to the results in Fig. 9.

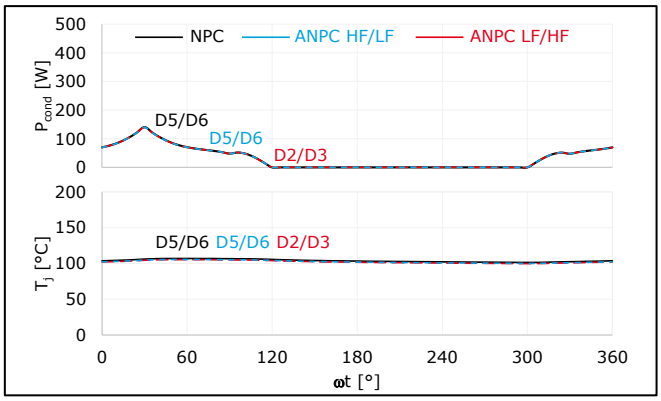


Fig. 14. Simulated power losses and junction temperature (average values) – inverter mode

For the operating mode energy storage the average conduction losses and the average junction temperature over an output period are shown in Fig. 15. The power losses of D1/D4 of the NPC and ANPC HF/LF as well as of D2/D3 of the ANPC LF/HF are identical. The losses in D5/D6 of the NPC are identical at pf=1 and -1. This can be seen from the comparison of Fig. 14 and Fig. 15. The diodes D5/D6 of the ANPC HF/LF are inactive at pf=-1 which is also consistent with the analytical expressions in Fig. 9.

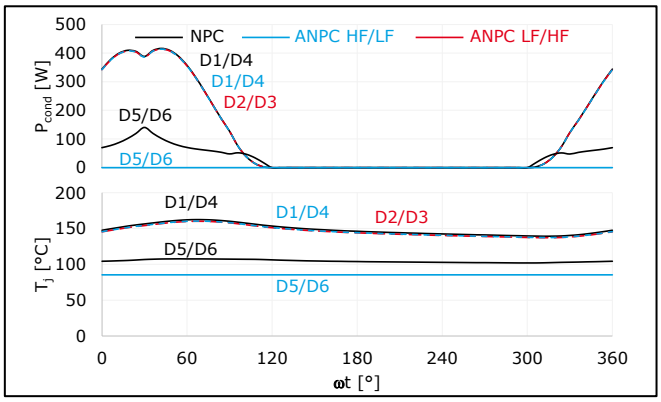


Fig. 15. Simulated power losses and junction temperature (average values) – energy storage

Based on the conditions shown in Fig. 16 the power losses and junction temperatures in case of LVRT are simulated (Fig. 17). Also in this case, the simulation result agrees with the analytical expressions in Fig. 9. In the NPC the diodes D5/D6 have the highest load that decreases with increasing modulation index. The load of the ANPC HF/LF also decreases with increasing output voltage. In the ANPC LF/HF, the current load is independent of the modulation index, which is reflected in the simulated power loss curve.

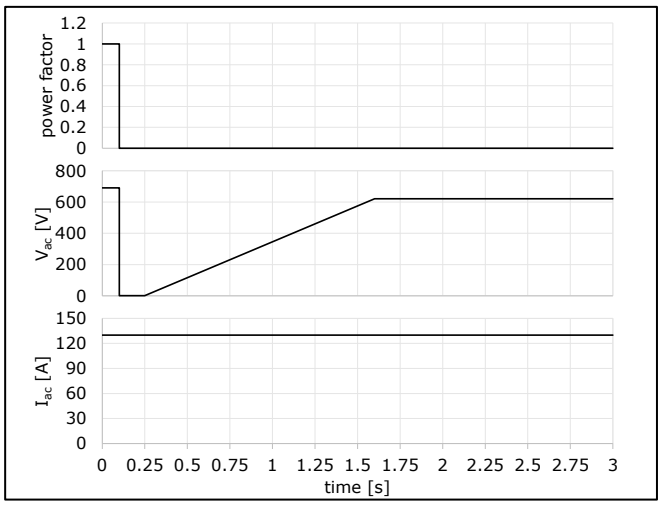


Fig. 16. Simulation conditions for LVRT

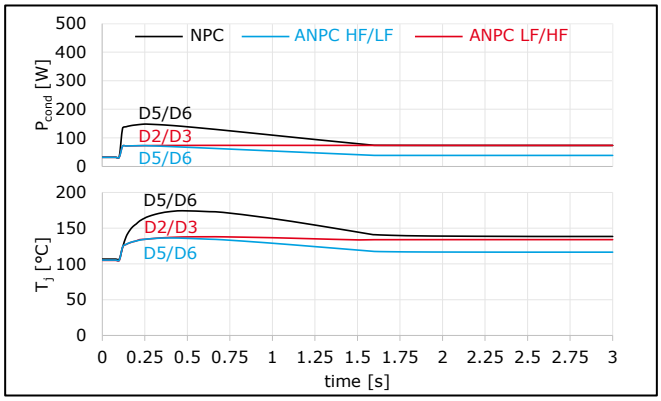


Fig. 17. Simulated power losses (average values) and junction temperature (peak ripple values) – LVRT

Although the simulation was performed with space vector modulation, the statements are consistent with the analytical results that have been derived assuming sine-triangle modulation.

8. Summary

In this paper the 3-Level topologies NPC and ANPC were considered under the aspect of Low Voltage Ride Through capability, use of SiC-SBD and the requirement for energy storage. Based on the individual diodes' current loads for each topology, an evaluation of the required SiC chip area was made for the respective operating mode. It became apparent that, in pure inverter mode (pf=1), the use of SiC area is the same for all

topologies. When more operating modes are required (inverter, LVRT, energy storage), more SiC area is required by the NPC and ANPC HF/LF topologies compared to the ANPC LF/HF. Provided that SiC remains more price-intensive than Si, the ANPC LF/HF then has a cost advantage.
The analytical expressions could be confirmed by simulation.
Furthermore, a potential realization for each topology was presented using standard 62mm half-bridge modules and evaluated with respect to the effort required to limit overvoltage.
For high output power based on high current single switch modules the ANPC LF/HF has the advantage of interleaved switching without parallel connection, which reduces the amount of higher harmonics at the same switching frequency.

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Appendix

The following expressions are used to calculate the average (avg) and RMS currents of the diodes D1/D4, D2/D3 and D5/D6 for the cases of NPC, ANPC HF/LF and ANPC LF/HF depending on the modulation index M and phase angle φ with 0≤φ≤π.
A sinusoidal output current $I_{out}(t) = \hat{I} \cdot \sin(2\pi f_{out} \cdot t)$ is assumed. The ripple current is neglected.

I_{avg}	NPC	ANPC HF/LF	ANPC LF/HF
D1/D4	$\frac{\hat{I}\,M}{4\pi} \cdot [\sin(\varphi) - \varphi\cos(\varphi)]$	$\frac{\hat{I}\,M}{4\pi} \cdot [\sin(\varphi) - \varphi\cos(\varphi)]$	$\frac{\hat{I}\,M}{4\pi} \cdot [\sin(\varphi) - \varphi\cos(\varphi)]$
D2/D3	$\frac{\hat{I}\,M}{4\pi} \cdot [\sin(\varphi) - \varphi\cos(\varphi)]$	$\frac{\hat{I}}{2\pi} \cdot [1 - \cos(\varphi)]$	$\frac{\hat{I}}{4\pi} \cdot [(2 - M\pi)\cos(\varphi) + 2]$
D5/D6	$\frac{\hat{I}}{4\pi} \cdot \left[4 + M\left((2\varphi - \pi)\cos(\varphi) - 2\sin(\varphi)\right)\right]$	$\frac{\hat{I}}{4\pi} \cdot [-M\sin(\varphi) + (M\varphi - M\pi + 2)\cos(\varphi) + 2]$	$\frac{\hat{I}}{4\pi} \cdot [-M\sin(\varphi) + (M\varphi - 2)\cos(\varphi) + 2]$

I_{rms}^2	NPC	ANPC HF/LF	ANPC LF/HF
D1/D4	$\frac{\hat{I}^2\,M}{6\pi} \cdot [\cos(\varphi) - 1]^2$	$\frac{\hat{I}^2\,M}{6\pi} \cdot [\cos(\varphi) - 1]^2$	$\frac{\hat{I}^2\,M}{6\pi} \cdot [\cos(\varphi) - 1]^2$
D2/D3	$\frac{\hat{I}^2\,M}{6\pi} \cdot [\cos(\varphi) - 1]^2$	$\frac{\hat{I}^2}{8\pi} \cdot [-\sin(2\varphi) + 2\varphi]$	$\frac{\hat{I}^2}{24\pi} \cdot [3\sin(2\varphi) - 16M\cos(\varphi) - 6\varphi + 6\pi]$
D5/D6	$\frac{\hat{I}^2}{12\pi} \cdot [3\pi - 4M(1 + \cos^2(\varphi))]$	$\frac{\hat{I}^2}{24\pi} \cdot [3\sin(2\varphi) - 2M\cos(2\varphi) - 8M\cos(\varphi) - 6\varphi - 6M + 6\pi]$	$\frac{\hat{I}^2}{24\pi} \cdot [-3\sin(2\varphi) - 2M\cos(2\varphi) + 8M\cos(\varphi) + 6\varphi - 6M]$